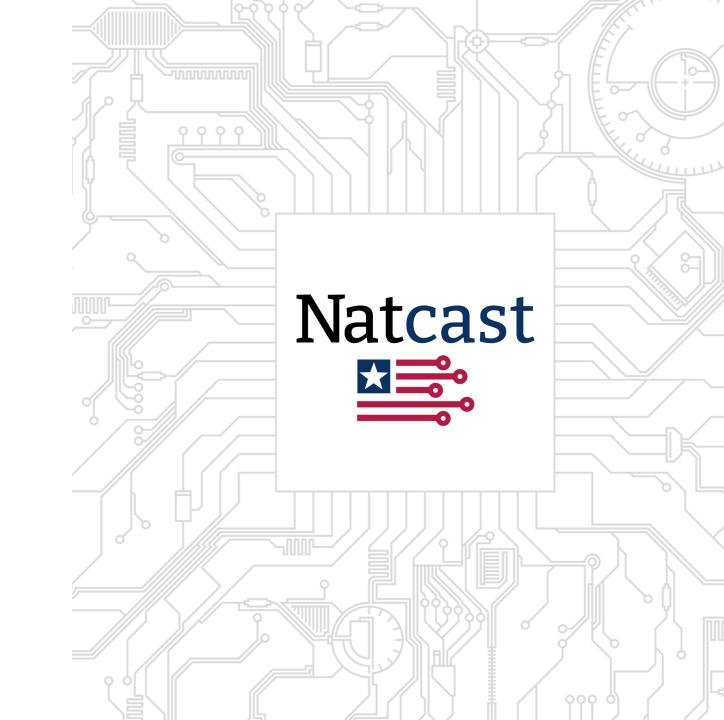


Natcast is the operator of the National Semiconductor Technology Center ("NSTC"). The NSTC is powered by CHIPS for America, funded by the Department of Commerce.

The views expressed in this publication are those of Natcast and do not necessarily reflect the views or positions of the federal government or NSTC members. CHIPS for America will further strengthen the domestic semiconductor industry, protect American national and economic security, preserve U.S. leadership in the industries of the future, create good-paying jobs, and build strong communities here in the United States. For more information, please visit chips.gov.

R&D PROJECT FUNDING: ARTIFICIAL INTELLIGENCE DRIVEN RF INTEGRATED CIRCUIT DESIGN ENABLEMENT (AIDRFIC)

June 21, 2024



# **Submit Your Questions**



Please submit your questions using the Zoom **Q&A** feature

?

All questions and answers will be posted to Natcast.org/research-and-development/AIDRFIC



### Disclaimer

Statements and responses to questions about advanced microelectronics research and development programs in this presentation:

- Are informational, pre-decisional, and preliminary in nature.
- Do not constitute a commitment and are not binding on NIST or the Department of Commerce.
- Are subject in their entirety to any final action by NIST or the Department of Commerce.

Nothing in this presentation is intended to contradict or supersede the requirements published in any future policy documents or funding opportunities.



# Today's Speakers



Deirdre Hanford
CEO
Natcast



**Greg Yeric, PhD**Director of Research
for the NSTC Program
CHIPS R&D Office



Ronald Gyurcsik, PhD
Acting Program Manager
Natcast

### Agenda

- CHIPS for America Vision
- Work of the NSTC and Natcast
- Overview of Research Strategy
- AIDRFIC Program Details, Eligibility, and Key Dates
- Proposers' Day Overview

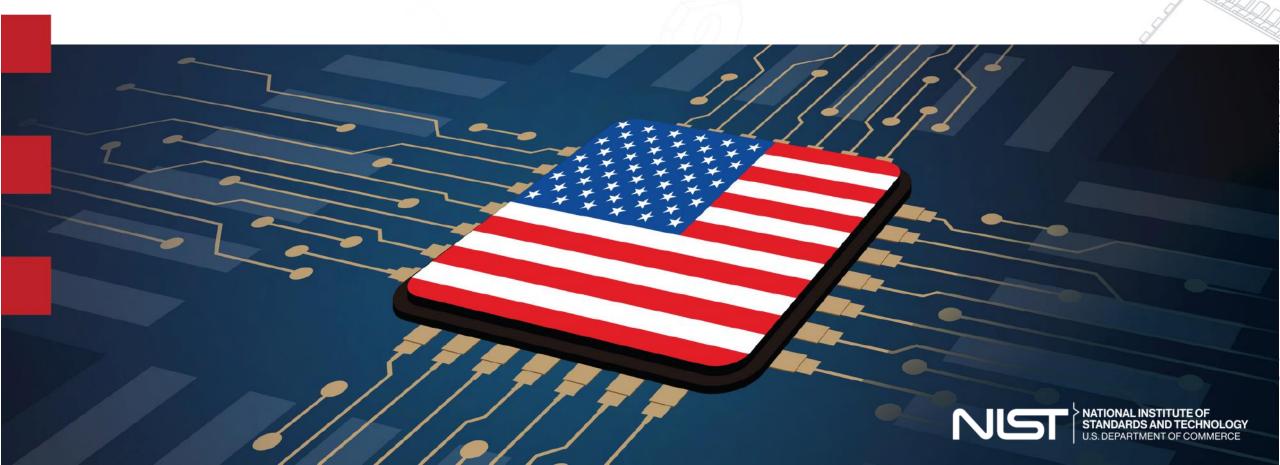
By the end of this webinar, attendees will better understand:

- Scope and schedule of the AIDRFIC program
- Key dates of the AIDRFIC program
- AIDRFIC Proposers'
   Day details



### CHIPS for America: Investment Overview





### The CHIPS & Science Act

### \$39B

#### **Incentives**

Invest in U.S. production of strategically important semiconductor chips, and assure a sufficient, sustainable, and secure supply of older and current generation chips for national security purposes and for critical manufacturing industries.

### \$11B

#### R&D

Strengthen U.S. semiconductor research and development (R&D) leadership to catalyze and capture the next set of critical technologies, applications, and industries.

### **\$2B**

#### **DoD**

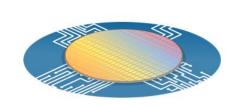
The DoD Microelectronics Commons is a national network that will create direct pathways to commercialization for US microelectronics researchers and designers from "lab to fab."

**Workforce Initiatives** 



# **CHIPS R&D Programs**





CHIPS National Advanced Packaging Manufacturing Program (NAPMP)



CHIPS Manufacturing USA Program



**CHIPS Metrology Program** 

**Workforce Initiatives** 



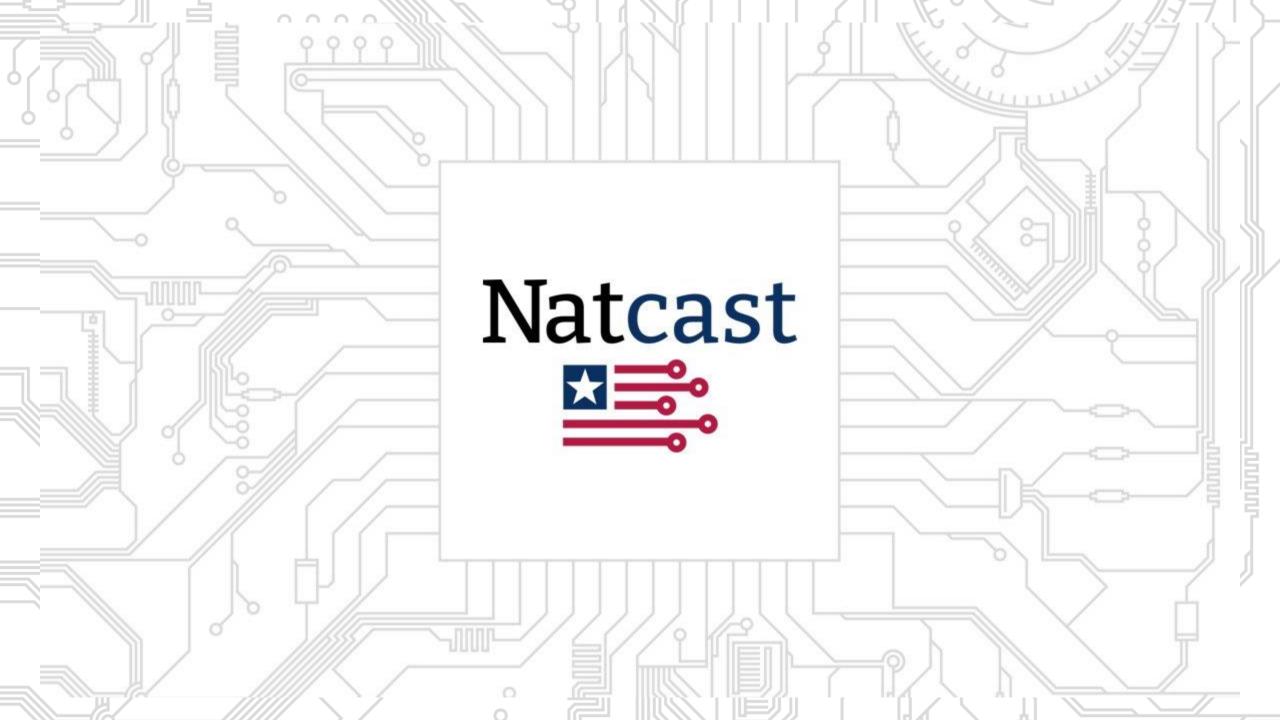
## **History & Progress**

#### **Engaging the Ecosystem** Published NSTC Vision & Strategy Natcast, a non-profit organization, 品 was independently established Engaged with thousands of **NSTC** Roadmap stakeholders and participated in public events 2023 May 2022 Jan-Apr 2024 **Establishing the NSTC Setting the Foundation** Anticipated \$5 billion investment CHIPS Legislation Passed Natcast selected as the NSTC operator Released an RFI Signed the consortium agreement Natcast launched the Community of Interest Hosted two public events with CHIPS & Natcast Natcast released RFI on Facilities & Capabilities

#### **Coming Up**

- Facilities Model and
  Selection Process
- Workforce Center of Excellence
- Opening Membership
- P Initial R&D Funding Opportunities ★





### **Focus Areas**



#### Research

Member-driven TAB

Research & Development Projects

Prototyping



# Lower Cost of Design

Design Enablement Gateway

Silicon Aggregation Services

Investment Fund



Technicians Regional

Engineers

Researchers



# NSTC to be a member-driven consortium that brings together a **diverse ecosystem**



Design



**Manufacturers** 



**Investors** 



**Academia** 



**End Customers** 



**Govt. Organizations** 



**Professional Services** 



Workforce Intermediaries



**Suppliers** 

Guiding Principles

Accessible

Valuable

Simple

Connected

Membership Opening Fall 2024



### The Road Ahead



**Facilities** 



Workforce **Development** 

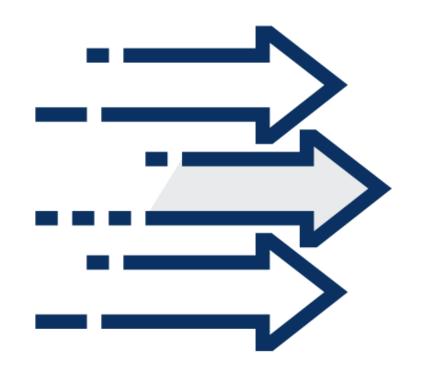


**Early Jump Start Projects** 



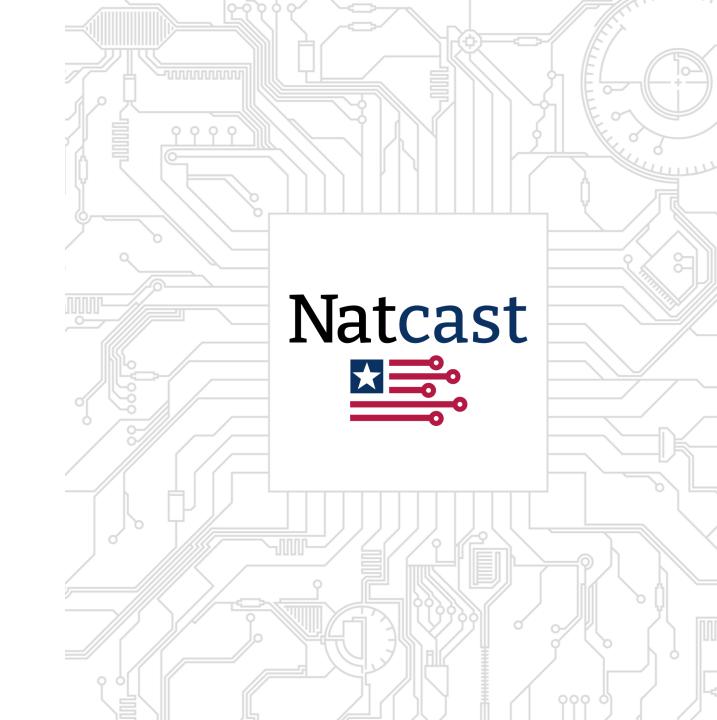
**Invite Members** 





# Early Jump Start Projects

Artificial Intelligence Driven RF Integrated Circuit Design Enablement (AIDRFIC)



# **Opening Disclaimer**

- The material in this webinar on the AIDRFIC program is pre-decisional and may evolve based on feedback and other considerations
- A call for proposals, once issued, will be the definitive source



### Reminder: Submit Your Questions



Please submit your questions using the Zoom **Q&A** feature

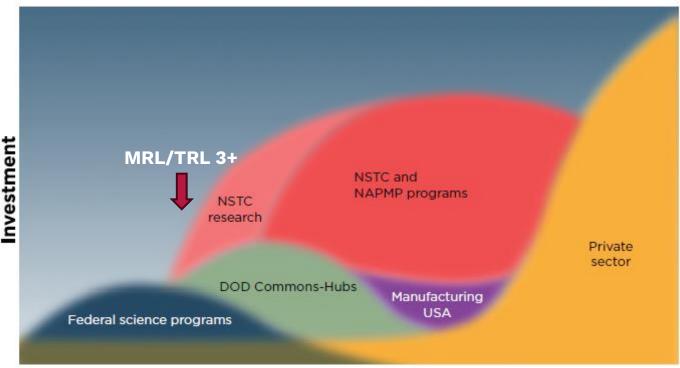


All questions and answers will be posted to Natcast.org/research-and-development/AIDRFIC



## **NSTC** Research Focus

**Goal:** Enhance and mature promising technologies (TRL 3+) developed by universities, USG labs or others, thus lowering investment risk for US Semiconductor companies.



**Technology Maturation** 

#### **Overall Investment Plan**

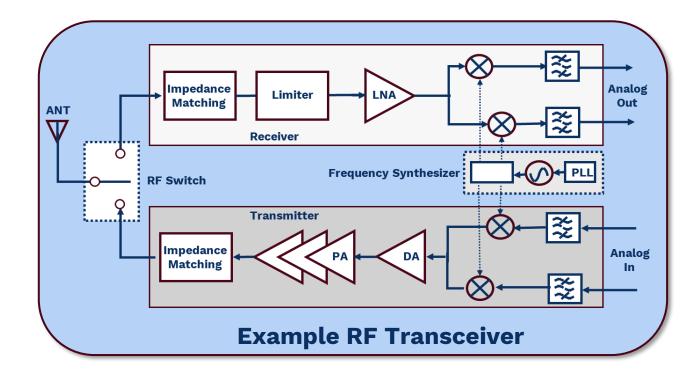
- > \$100M Initial Investment
- 4-5 research topics over next
   6 months; next 2 topics:
  - Test Vehicles
  - PFAS (under consultation)
- Project lengths up to 30 months

Image source: April 2023 NSTC Vision document



### RFICs Are Everywhere

- Wireless communication and connectivity: integrated across many commercial applications and growing daily
- Automotive radar systems: transforming the way we drive and improving safety
- Wireless sensor networks: flexible and scalable, utilized across automation, security, and monitoring
- Satellite communication: providing signal amplification, frequency conversion, and modulation for communication and sensing



RF Circuit building blocks such as PAs, LNAs, Mixers, PLLs, switches, and impedance matching networks are common to many RF systems.



# Why AIDRFIC?

#### **Observations**

- The growth and adoption of AI technology is transforming the way we live and work
- RFICs are key to an ever-increasing number of commercial, industrial, and defense systems

#### Challenge

- Productivity of RF circuit design has not kept pace
- Limited workforce

#### Goals

- Lower the experience barrier to design RF Integrated Circuits
- Increase RFIC design productivity
- Optimize RFIC designs
- Generate unique, non-intuitive RFIC designs



### **AIDRFIC Focus**

- Well understood design flow
- Iterative design
- Circuit Design, Physical Design and System Verification targeted
- Addresses program goals
- Supports greater exploration at system level

#### **RF Design Flow**

_			
	Design Specifications	<ul> <li>Performance specifications</li> <li>Physical and electrical constra</li> <li>System topology</li> </ul>	aints
	System Design	<ul><li>High-level design</li><li>Behavioral modeling</li></ul>	
	Circuit Synthesis	<ul><li>Mixed-level simulation</li><li>Functional partitioning</li></ul>	
	Circuit Design	<ul><li>Foundry design kit</li><li>Passive device modeling</li><li>Detailed circuit design</li></ul>	
	Physical Design	<ul> <li>Layout</li> <li>EM simulation and extraction</li> <li>Parasitic extraction</li> <li>DRC</li> <li>LVS</li> </ul>	
	System Verification		
	Tape-out		



# Task 1: Create training set and baseline performance data

- Develop training set
- Share training set with other teams
- Determine baseline productivity data

- Training set a Deliverable to Natcast
- Option to choose either a given Si/SiGe or GaAs process
  - GaAs exemplars at microwave frequencies
  - Si/SiGe exemplars at millimeter wave frequencies
- GaAs chosen due to broad availability and use within the commercial sector



# Task 2: Update tools and integrate into an AI-based RFIC design flow

- Update tools
- AI-enabled tools should be able to perform "inverse" goal-driven design
- Demonstrate the capability to learn through training and/or use

- Address sensitivity to layout and process variations
- Detect and flag erroneously generated results
- Tools and methodology should be process independent



#### **Task 3: Demonstrate updated tools**

- Use AI-enabled tools to design two RF circuits with Natcast supplied specifications
- Compare performance of generated circuits to exemplar specifications
- Document approach and tools
- Detail strengths and weaknesses

- Natcast will provide initial exemplar RF circuit specifications
- Demonstrate capabilities of tools



# Task 4: Refine AI-enabled tools, benchmark results, and validate performance

- Use AI-based design tools to design up to 5 additional RF circuits and populate a shared test wafer
- Submit designs for considered inclusion on shared wafer run
- Fabricated ICs tested and validated by independent third party

- Natcast will provide the specifications for additional exemplars derived from real-world systems
- There will be five Si/SiGe millimeter wave specifications and five GaAs microwave specifications



# Task 5: Document and integrate into RF design courses

- Identify learnings from the AIDRFIC project most relevant to academic curriculum or a workforce training program
- Identify a suitable class or training and develop a plan to integrate
   AIDRFIC learnings into the training

# Task 6: Develop a business plan to commercialize technology

- Publish or patent the results of the AIDRFIC project, as appropriate
- Develop a technology transition plan to commercialize the technology and make it available
- Document expected commercial, economic, and national security benefits to the United States

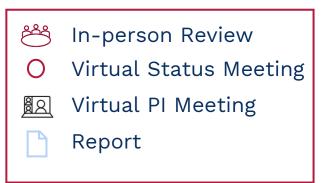


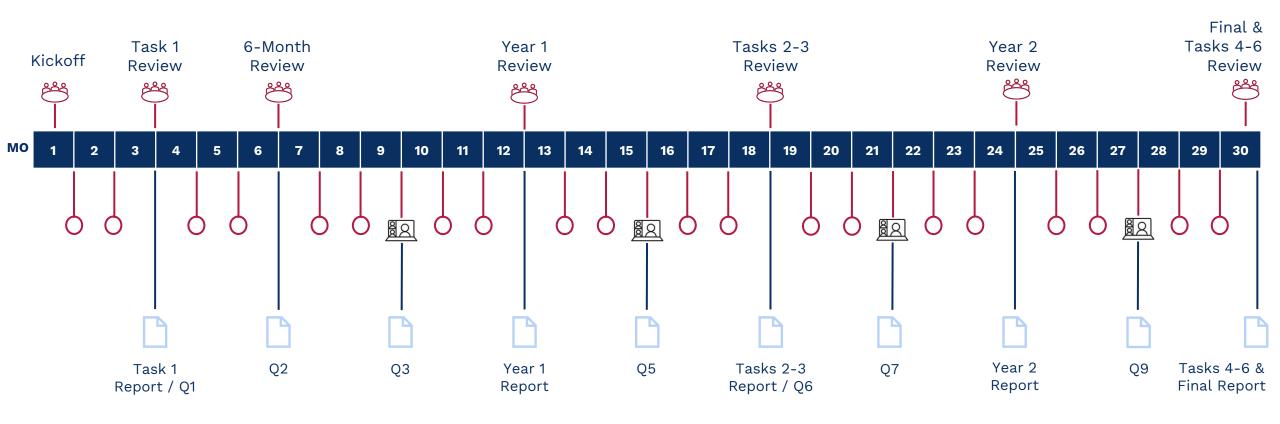
# Task Timeline

Task 1	Training set and baselines					
Task2	Update Tools and Integrate into an AI-based RFIC design flow					
	Demonstrate Updated tools					
Task 3	Independent Verification of exemplars					
	Benchmark updated tools using system driven design specifications					
Task 4	Independent RF test  Tape-out					
Task 5	Document and Integrate into academic RF design courses					
Task 6	Document a plan to commercialize the technology					
	<b>Start</b> Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 End					



# Al for RF Schedule *AIDRFIC*







# **AIDRFIC** Details and Key Dates

- Anticipated Amounts: Total program funding up to \$30M with 3-4 awardees anticipated
- Eligibility: Natcast members at the time of award. Must be eligible to become Natcast members to propose
- Cost Sharing Requirements: None
- Teaming Opportunities: Proposers'
   Day will facilitate teaming on
   July 11, 2024. Teams encouraged to
   start discussions prior to 7/11

#### **Key Dates**

**Call for Proposals Released** 

**Proposers' Day** 

**Executive Summary Due** 

**Proposals Due** 

**Target Awards Announced** 

**Target Project Start** 

June 28, 2024\*

July 11, 2024

July 25, 2024

**August 16, 2024** 

**October 17, 2024** 

**December 2, 2024** 

\*Target



# Proposers' Day Agenda\*

7:30 - 8:30	Registration/coffee
8:30-8:40	Introductory remarks
8:40-9:30	DOC & Natcast Overview
9:30-10:20	RF design challenges of today and tomorrow panel session
10:20-10:40	Break
10:40-11:30	Potential of AI in RF IC design panel session
11:30-12:00	AIDRFIC Program overview
12:00-1:00	Lunch (on site)
1:00-2:15	5-10min presentations by researchers who have demonstrated use of AI in RF design
2:15-2:30	Break
2:30-3:15	3-5min presentations by entities that could function as team members
3:15-4:15	Informal breakout sessions for teaming discussions
4:15-4:45	Submission and evaluation process
4:45-5:00	Wrap-up

\* Subject to change

When:

Thursday, July 11, 2024

Where:
Hilton
Arlington

**Details:** 

To be posted to Natcast.org



# Intellectual Property (IP) and Data Rights

#### All proposers must identify

- Pre-existing IP used to complete the project
- o IP that may be developed with Natcast funding if awarded

#### Proposals must include an Intellectual Property Management Plan that

- Commits a government patent license to patentable foreground IP & government data rights for government purposes in reported information
- Grants Natcast a sublicensable license to developed IP and performance data for noncommercial purposes
- Offers additional proposer-defined IP benefits to the NSTC membership and/or to advance domestic production



### Teaming

#### Teams are expected to include a subset of

- University researchers (R&D, training and workforce development)
- Commercial RF and defense companies (RF design)
- Si/SiGe and/or compound semiconductor foundries (Foundries)
- Established and/or start-up EDA tool companies (EDA tools and flows, commercialization)
- US government funded labs (RF design, Foundries)



# Fully Addressed at Proposers' Day

#### **July 11th – Hilton Arlington**

- Fundamental research definition and implications
- Research security
- Commercial viability and domestic production
- Evaluation, selection criteria and review process
- Meeting and reporting schedule
- Budget format and payment terms



# Proposers' Day – July 11<sup>th</sup> Please Respond With Your Interest by June 28<sup>th</sup>

#### **Panel Members and Moderators Needed**

- o RF design challenges of today and tomorrow panel session
- o Potential of AI in RF IC design panel session

#### **Presentations by Interested Team Leaders and Participants**

- o 5-10min presentations by researchers who have demonstrated use of AI in RF design
- o 3-5min presentations by entities that could function as team members

#### **Proposal Reviewers Pool Members**

Foundries interested in fabricating multi-project wafers

Please respond to Ron Gyurcsik at AIDRFIC2024@natcast.org

All Proposers' Day details and signup at Natcast.org/research-and-development/AIDRFIC



## Thank You!



Sign up for our email newsletter at <u>Natcast.org</u>

