CHIPS for America and Natcast Processes to Select Three R&D Facilities

Model for the First Three CHIPS for America R&D Facilities

On July 12, 2024, the Department of Commerce and Natcast, the operator of the National Semiconductor Technology Center (NSTC), announced the model for the first three CHIPS for America Research and Development (R&D) facilities for the NSTC and National Advanced Packaging Manufacturing Program (NAPMP):

- NSTC Administrative and Design Facility
- NSTC Extreme Ultraviolet (EUV) Center
- NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility

These three state-of-the art facilities will establish world-class destinations for advanced semiconductor R&D in the United States. They will address critical gaps in the current ecosystem, offering unparalleled value to a diverse array of stakeholders across the semiconductor value chain, including universities, businesses of all sizes, and government agencies. The Department and Natcast intend for the NSTC Administrative and Design Facility to be operational in 2025, the NSTC EUV Center by 2026, and the NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility in 2028.

Together, these facilities will allow the brightest minds to collaborate and solve the most challenging problems in microelectronics. Specifically, these first three facilities will:

- **Accelerate innovation** by enabling world class R&D across the full range of microelectronics technical areas—including access to EUV lithography, which is needed for research using the most advanced patterning technology;
- **Create differentiation** to ensure there is a clear value to the semiconductor ecosystem beyond existing comparable facilities;
- **Be financially sustainable** by creating enduring value for decades and attracting investment from all types and sizes of companies;
- **Be independent and neutral** by enabling Natcast, on behalf of the NSTC, and the NAPMP to make strategic decisions about the operation of the facilities, and by ensuring that the facilities are places where all member entities and their employees have the opportunity to successfully innovate;
- **Exist in thriving and vibrant ecosystems** that can provide, foster, and grow a talented workforce and a robust ecosystem of semiconductor companies, educational and research institutions, and local support to advance the mission.

As described in more detail in the facilities model, these are the first three foundational facilities in what are envisioned to become an integrated network of facilities that will provide capabilities, services, and mission-enabling support for CHIPS for America.

The Department and Natcast will pursue three separate site selection processes—one for each facility—given the varying timelines and technical specifications of each. These three investments will work together to create long-term and sustainable value for the entire domestic semiconductor ecosystem. The Department and Natcast will select facilities deemed the most advantageous to the objectives of CHIPS for America, including based on an integrated assessment of all the factors considered in each selection process.

The Department and Natcast expect additional facility capabilities will be needed over time, including those via affiliated technical centers. Additional facilities capabilities will be identified and prioritized as the NSTC continues to mature.

This document explains the processes that the Department and Natcast will use to select the first three facilities.

NSTC Administrative and Design Facility

The NSTC Vision outlines a clear vision of a place-based institution for research and ecosystem convenings. The NSTC Administrative and Design Facility will be a multi-functional facility, serving as the location for key operations of the NSTC, including: hosting Natcast administrative functions; convening consortium members; and conducting NSTC programmatic activity such as the Workforce Center of Excellence and the NSTC Design Enablement Gateway.

The NSTC Administrative and Design Facility will have a heightened focus on the semiconductor design ecosystem. The facility will require access to semiconductor design, electronic design automation (EDA), and semiconductor workforce expertise, as well as administrative and corporate talent. In addition, proximity to universities with advanced microelectronics research is essential.

The NSTC Administrative and Design Facility selection process will be run by Natcast with support from a site selection firm that brings significant commercial experience in selecting facilities, including in the semiconductor industry. This facility must be located in a region with a thriving and vibrant semiconductor ecosystem, with a special focus on semiconductor design ecosystems and other required functionality. It is expected that this will be a leased facility housing up to 150 employees, as well as researchers, partners, academics, and suppliers in its early years. Natcast will also utilize best practices from commercial site selection processes and has designed a process to efficiently identify the most viable sites with the objective that the facility will be occupied and operational in 2025.

Phase 1 – Identification of Semiconductor Design Ecosystems

Natcast will use a variety of data resources to evaluate states, regions, and metro areas against the NSTC Administrative and Design Facility specifications to determine a short list of regions that best match requirements. NSTC Administrative and Design Facility specifications include corporate office capabilities, specifically considering:

- **Semiconductor Design Ecosystem**: The presence and planned growth of a semiconductor design ecosystem within a region/metro area:
    - **Semiconductor Industry Value Chain**: The number and caliber of semiconductor companies present and active in an area. Though focused on design, this also includes other areas of the value chain like materials, capital equipment, and manufacturing/packaging;
    - **Semiconductor Workforce**: The number of people currently working in the semiconductor field. Though focused on the design workforce, this also includes other areas of the value chain like materials, capital equipment, and manufacturing/packaging;
    - **Top Research Universities (R1 Universities) focused on Microelectronics**: The number and caliber of university research and advanced degree programs focused on microelectronics.

- **Access to Relevant Functionality and Services**: Ease of travel and access to various critical spaces and activities that support the facility's mission, such as:
    - Convening/conference space to host a large population of semiconductor researchers and conference attendees;
    - Research universities with strong semiconductor/microelectronics programs; and
    - Other potential semiconductor ecosystems.

Phase 2 – Identification of Locations, Due Diligence, and Negotiations

Once regions/metropolitan areas with advantageous semiconductor design ecosystems have been identified, Natcast will contact Economic Development Organizations (EDOs) in those states and/or territories to provide proposed sites/facilities.

Natcast will invite the most viable sites to participate in due diligence and negotiations. Natcast will visit the proposed most viable sites and meet with relevant stakeholders to address the site/facility characteristics, costs, timeline, and partnership opportunities.

The information gathered during the various analyses and visits—as well as the availability of state and local incentives—will inform Natcast's determination of which sites it will invite to participate in final negotiations. Natcast expects that a very small number of sites will be invited to participate in final negotiations for the NSTC Administrative and Design Facility. The Department and Natcast will select the site deemed the most advantageous to the objectives of CHIPS for America.

NSTC EUV Center

The NSTC EUV Center will provide NSTC members with access to EUV technology to facilitate a wider range of research and a path to commercialization, including technologies with the most challenging feature sizes. Next-generation technology development requires access to EUV lithography. Promising technologies that will be used in the most advanced logic or memory technology nodes must be evaluated and developed at length scales at or beyond the state of the art, and these can only be achieved today using EUV lithography tools.

Criteria and Process

Given the high costs of purchasing and maintaining EUV tools and the goal to provide access to these capabilities as soon as possible, Natcast will initially obtain access to EUV lithography for the NSTC through an agreement with an existing facility that meets the NSTC program requirements. Natcast will manage the selection process for the NSTC EUV Center in partnership with the Department. There are a limited number of existing U.S. entities who can provide the EUV capabilities described above. Accordingly, the Department and Natcast anticipate inviting only those entities with the necessary technical capabilities to participate in a selection and negotiation process. The Department and Natcast will select a facility deemed the most advantageous to the objectives of CHIPS for America and expect it to be operational in an existing facility by no later than 2026.

NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility

To achieve the ambitious goal of providing 300mm research, prototyping, and packaging capabilities in a single location that is ultimately financially sustainable, the NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility must be located in a region with a thriving and vibrant semiconductor ecosystem. The NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility will combine prototyping for state-of-

the-art manufacturing and packaging and next-generation technology development. Semiconductor manufacturing and packaging is complicated and expensive, and requires substantial investments, highly specialized spaces, elaborate tooling and equipment, and a complex supply chain of materials to sustain these operations. These capabilities require a skilled, experienced workforce to operate the facility, manage baseline technology flows, and maintain the equipment. Next-generation technology development requires a community of researchers, scientists, engineers, and technicians that can imagine and implement technologies beyond the state of the art. Prioritizing a thriving and vibrant semiconductor ecosystem for the NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility ensures that both the NSTC and NAPMP programs can attract participation from the people and companies that are needed to make this a worldwide center of gravity for collaborative semiconductor research.

To achieve the vision of the NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility, the Department and Natcast will conduct a multi-phase site selection process, initially focused on identifying semiconductor ecosystems, followed by a site-specific search. Natcast will work directly with the EDOs in each state and territory to facilitate the selection process. Natcast will manage the process in partnership with the Department, and with support from a site selection firm that brings significant commercial experience in selecting facilities, including in the semiconductor industry.

Phase 1 – Semiconductor Ecosystem Assessment

The Department and Natcast will issue an "Ecosystem Questionnaire for States and Territories to Inform CHIPS R&D Facility Site Selection Process" (Ecosystem Questionnaire) to the EDOs of all 56 states, territories, and the District of Columbia to identify thriving and vibrant semiconductor ecosystems that could potentially support the NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility. Participation by EDOs in the Ecosystem Questionnaire is voluntary. However, states and territories must complete the Ecosystem Questionnaire, through their respective EDOs, in order to be considered for the NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility.

The information provided by the EDOs is subject to further verification and clarification. The states' and territories' responses to the Ecosystem Questionnaire, in addition to other data sources, will inform the Department and Natcast's determination as to which states and territories have a thriving and vibrant semiconductor ecosystem that could best support the NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility.

The Department and Natcast will consider the following factors as they seek to identify the best semiconductor ecosystems:

- **Industry Presence**: The presence and planned growth of the semiconductor value chain, such as commercial semiconductor fabrication plants, advanced semiconductor packaging facilities, semiconductor equipment and material suppliers, and semiconductor design companies;
- **Availability of Workers**: The number of people currently working in semiconductor design, manufacturing, or closely-related fields and types of expertise;
- **Advanced Microelectronics Education and Research**: The number and caliber of university research and advanced degree programs focused on microelectronics;
- **Workforce Development**: The number and quality of semiconductor-focused training programs;
- **Investment**: The amount of private and public investments in the semiconductor industry in the previous decade;

- **State/Territory Support**: The number and type of benefits, incentives, and/or initiatives that benefit the semiconductor industry.

Given these unique ecosystem features, the Department and Natcast expect only a limited number of states and territories to possess a thriving and vibrant semiconductor ecosystem capable of hosting this facility.

Phase 2 – Site Evaluation

Phase 2 will allow invited states and territories to provide detailed information about specific proposed sites for the NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility in their state or territory, such as:

- **Real Estate and Infrastructure**: The characteristics of the specific real estate proposed, including alignment to physical and technical specifications provided by Natcast and the Department; environmental factors; and the existence of certain utilities and other infrastructure;
- **Costs**: The key estimated one-time and operating costs for the facility;
- **Operating Environment**: The anticipated timing to achieve buildout and full-scale operations and potential operating risks for the specific site and location;
- **Non-Federal Support**: The extent and level of non-federal support such as state and local incentives and private capital;
- **Proposed Partnership Approach**: Proposed partnerships with entities (e.g., companies, universities, research organizations, workforce providers, state and local governments) in the region to support the mission; and
- **Site-Specific Semiconductor Ecosystem Attributes**: Whether the site will sufficiently benefit from the thriving and vibrant semiconductor ecosystem in the state or territory.

The Department and Natcast expect to evaluate site-specific information provided by states and territories; additional information that may be gathered during potential site visits; initial discussions regarding state and local incentives; and other data sources in order to determine which sites will be invited to participate in final negotiations for this facility. The Department and Natcast anticipate that a very small number of sites will be invited to participate in final negotiations, which are expected to include ongoing due diligence by the Department and Natcast, as well as opportunities for states and municipalities to offer financial and other incentives. The Department and Natcast will select the site deemed the most advantageous to the objectives of CHIPS for America.

How to engage

If you have questions regarding these opportunities, please email FacilitiesRFI@natcast.org. An FAQ will be maintained at natcast.org/facilities.

Proposals received outside of the processes described above will not be evaluated.