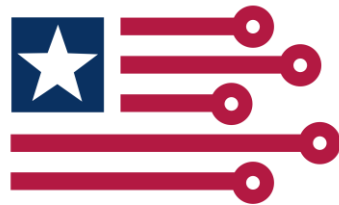


Natcast



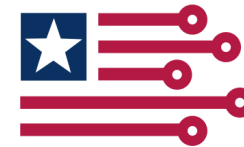
Natcast is the operator of the National Semiconductor Technology Center (“NSTC”). The NSTC is powered by CHIPS for America, funded by the Department of Commerce.

The views expressed in this publication are those of Natcast and do not necessarily reflect the views or positions of the federal government or NSTC members. CHIPS for America will further strengthen the domestic semiconductor industry, protect American national and economic security, preserve U.S. leadership in the industries of the future, create good-paying jobs, and build strong communities here in the United States. For more information, please visit chips.gov.

R&D PROJECT
FUNDING: TEST
VEHICLE INNOVATION
PIPELINE (TVIP)

August 21, 2024

Natcast



Submit Your Questions



Please submit your questions using the Zoom Q&A feature



Responses to questions will be posted to [Natcast.org/research-and-development/TVIP](https://natcast.org/research-and-development/TVIP) at a later date

Disclaimer

Statements and responses to questions about the TVIP Program, and any other material covered today:

- Are informational, pre-decisional, and preliminary in nature and may evolve based on feedback and other considerations.
- Do not constitute a commitment and are not binding on Natcast, NIST or the Department of Commerce.
- Are subject in their entirety to any final action by NIST or the Department of Commerce.

The TVIP Call for Proposals, once issued, will be the definitive source for the TVIP Program.

Today's Speaker



Brian D. Hoskins, Ph.D.
Program Manager, Test Vehicles
Natcast

Agenda

- CHIPS for America Vision
- Work of the NSTC and Natcast
- Overview of Research Strategy
- TVIP Program Details, Eligibility, and Key Dates
- Proposers' Day Invitation

By the end of this webinar, attendees will better understand:

- *Scope and schedule of the TVIP program*
- *Key dates of the TVIP program*
- *TVIP Proposers' Day*

The CHIPS & Science Act

\$39B

Incentives

Invest in U.S. production of strategically important semiconductor chips, and assure a sufficient, sustainable, and secure supply of older and current generation chips for national security purposes and for critical manufacturing industries.

\$11B

R&D

Strengthen U.S. semiconductor research and development (R&D) leadership to catalyze and capture the next set of critical technologies, applications, and industries.

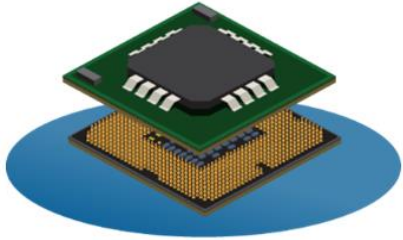
\$2B

DoD

The DoD Microelectronics Commons is a national network that will create direct pathways to commercialization for US microelectronics researchers and designers from “lab to fab.”



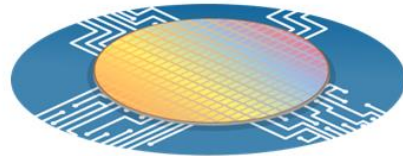
CHIPS R&D Programs



CHIPS National Semiconductor Technology Center (NSTC) Program

Natcast 

Natcast is an independent nonprofit organization and operator of the NSTC consortium



CHIPS National Advanced Packaging Manufacturing Program (NAPMP)



CHIPS Manufacturing USA Program



CHIPS Metrology Program



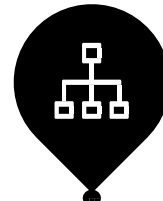
NSTC Roadmap: 4 Year View

- ✓ Facilities Model and Selection Process
- ✓ Workforce Partnership Alliance Program
- ✓ NSTC initial R&D funding call for proposals for AI-based RF design
- ✓ NSTC R&D Proposers' Day for AIDRFIC
- ☐ R&D funding call for the Test Vehicle Innovation Pipeline

Engaging the Ecosystem

- ✓ Published NSTC Vision & Strategy
- ✓ Natcast, a non-profit organization, was independently established
- ✓ Engaged with thousands of stakeholders and participated in public events

2023



NSTC Roadmap

May

Summer

Fall

Growing the NSTC

- ☐ Additional member services introduced

2025

2022

Setting the Foundation

- ✓ CHIPS Legislation Passed
- ✓ Released an RFI



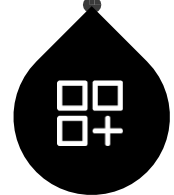
Jan-Apr 2024

Establishing the NSTC

- ✓ Anticipated \$5 billion investment
- ✓ Natcast selected as the NSTC operator
- ✓ Signed the consortium agreement
- ✓ Natcast launched the Community of Interest
- ✓ Hosted two public events with CHIPS & Natcast
- ✓ Natcast released an RFI on Facilities and Capabilities

★ We are
HERE

- ☐ Update on Facilities Search
- ☐ NSTC R&D Proposer's Day for TVIP
- ☐ Open Membership



NSTC to be a member-driven consortium that brings together a **diverse ecosystem**



Design



Academia



Professional Services



Manufacturers



End Customers



Workforce Intermediaries



Investors



Govt. Organizations



Suppliers

Guiding Principles

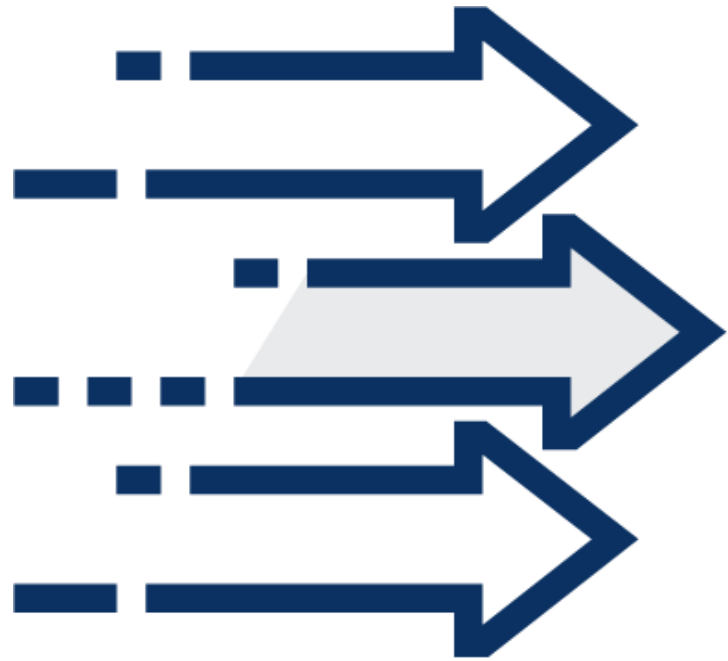
Accessible

Valuable

Simple

Connected

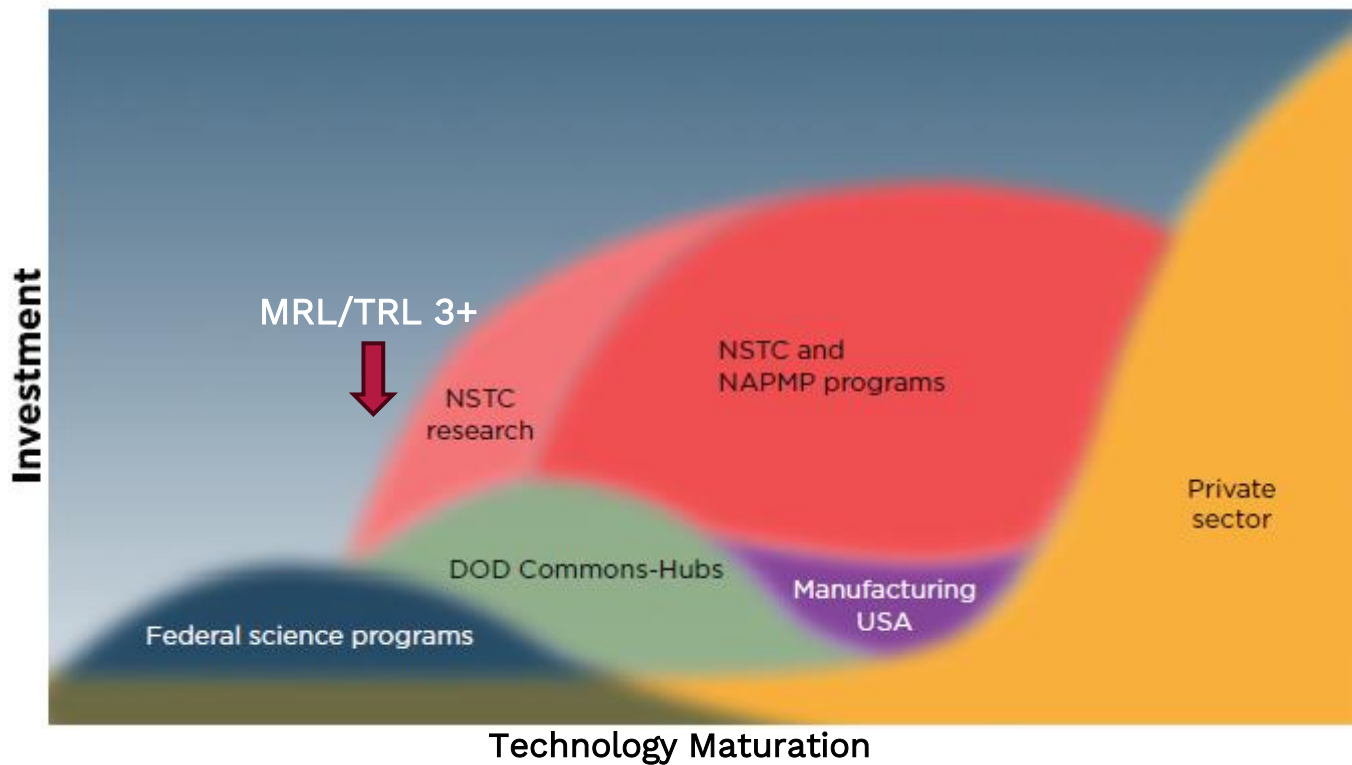
Membership Opening
Fall 2024



Early Jump Start Projects

NSTC Research Focus

Goal: Enhance and mature promising technologies (TRL 3+) developed by universities, USG labs or others, thus lowering investment risk for US Semiconductor companies.



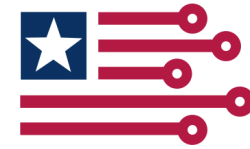
Overall Investment Plan

- > \$100M Initial Investment
- 4-5 research topics over next 6 months;
- Previous Topic:
 - AIDRFIC
- Upcoming Topic:
 - PFAS Abatement
- Project lengths up to 30 months

Image source: April 2023 NSTC Vision document

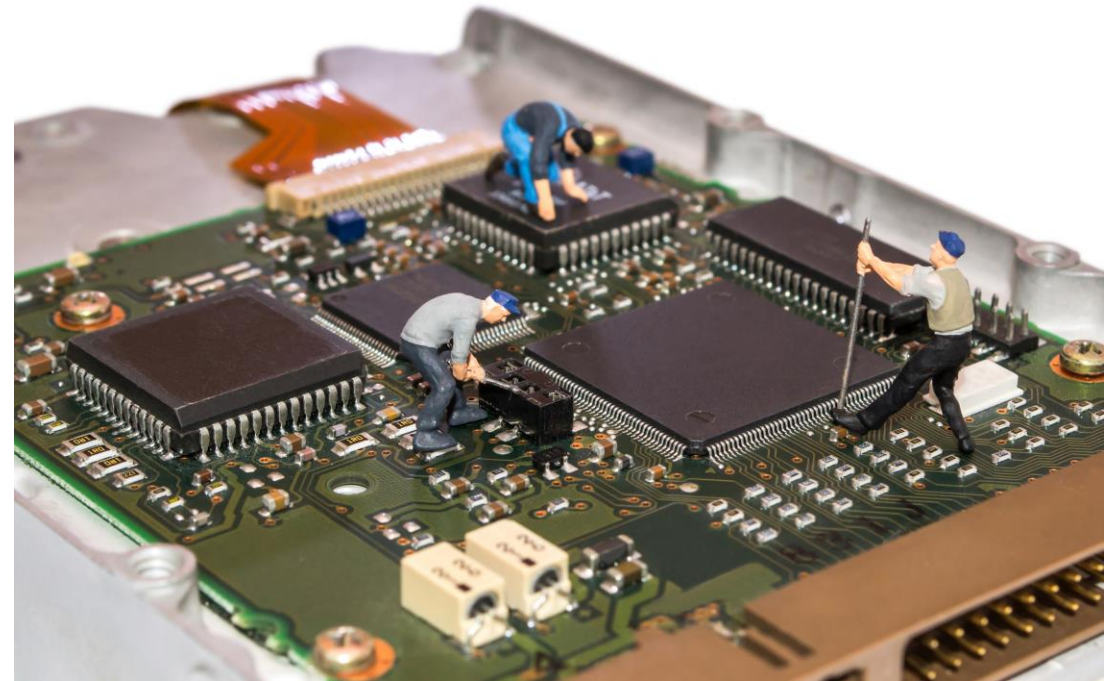
Test Vehicle Innovation Pipeline (TVIP)

Natcast



Hardware is hard.

- **The costs of research and development are rising:** the number of leading-edge companies has steadily fallen over past 20 years
- **Investments are risky:** investing in the “wrong technology” can put you behind years, disrupt production lines
- **Supply chains are rigid:** flows, processes, and materials are fixed to existing high-volume manufacturing
- **Cycles times are long:** 3-4 months to deliver new results from a full flow manufacturing process. Debug can take a year



Credit: iStock.com/Luda311

Why the Test Vehicle Innovation Pipeline?

Observations

- The capital costs of semiconductor research are rising dramatically
- Transitioning new technologies into a production fab comes with significant risks from opportunity cost and material compatibility

Opportunities

- Providing standardized Test Vehicles for diverse stakeholders can eliminate large Non-Recurring Engineering Costs (NREs)
- Introducing industrially derived Test Vehicles earlier in R&D can help benchmark performance and mitigate materials compatibility issues

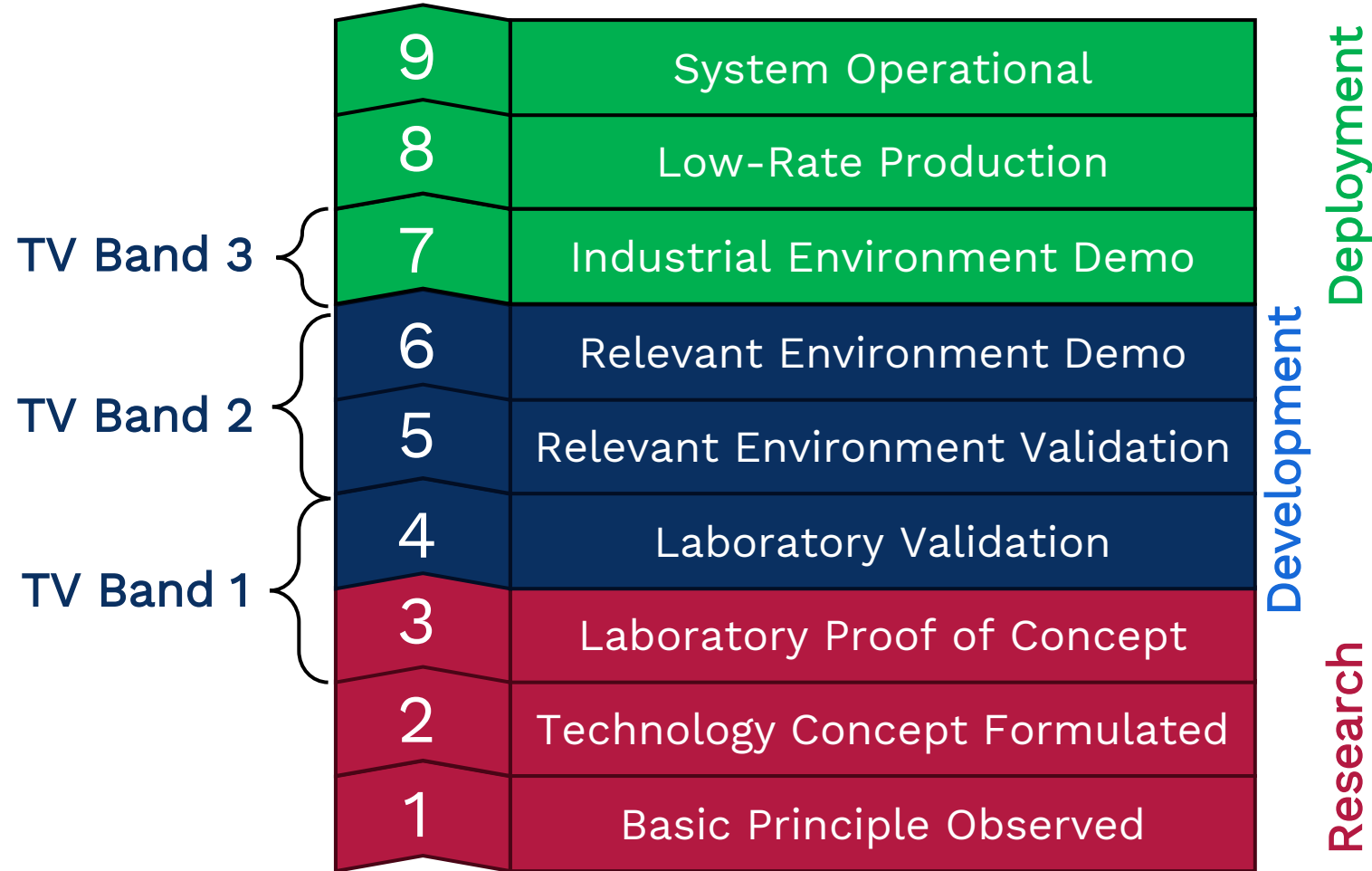
Goals

- Provide NSTC members silicon proven Test Vehicles for use in research facilities sourced from major fabrication facilities like a commercial foundry
- Provide incremental pathways from labs into facilities that can help process Test Vehicles with robust baseline flows for prototyping
- Use data to address performance and materials/process compatibility

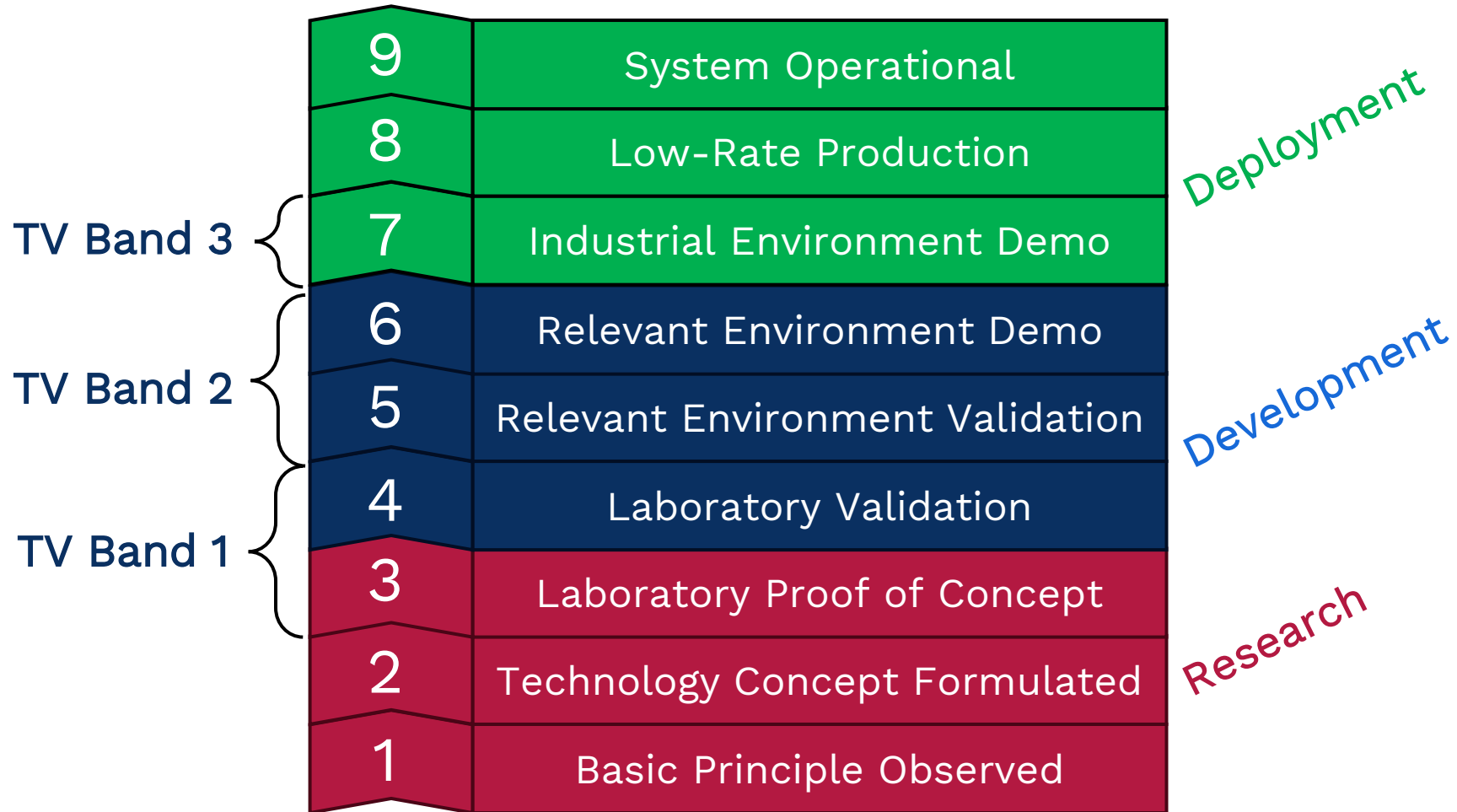
TRLs for TVIP

- TRLs have a definition based on the environment in which work is performed
- Test Vehicles introduced into each environment must be appropriate for the user and toolsets
- Projects should envision success: one Test Vehicle from one TRL should build on the next
- Research at one TRL should be able to be reproduced in the next using common Vehicles

Technology Readiness Levels (TRL)



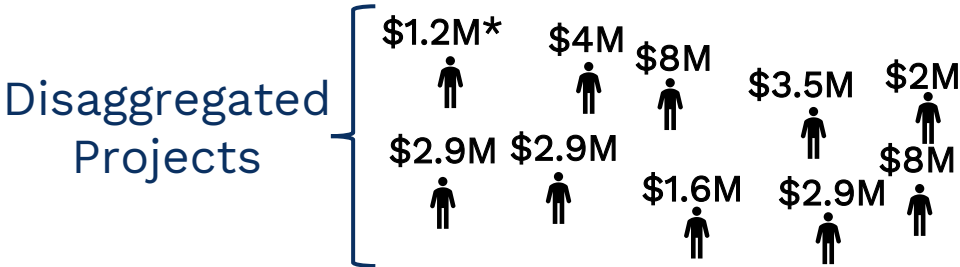
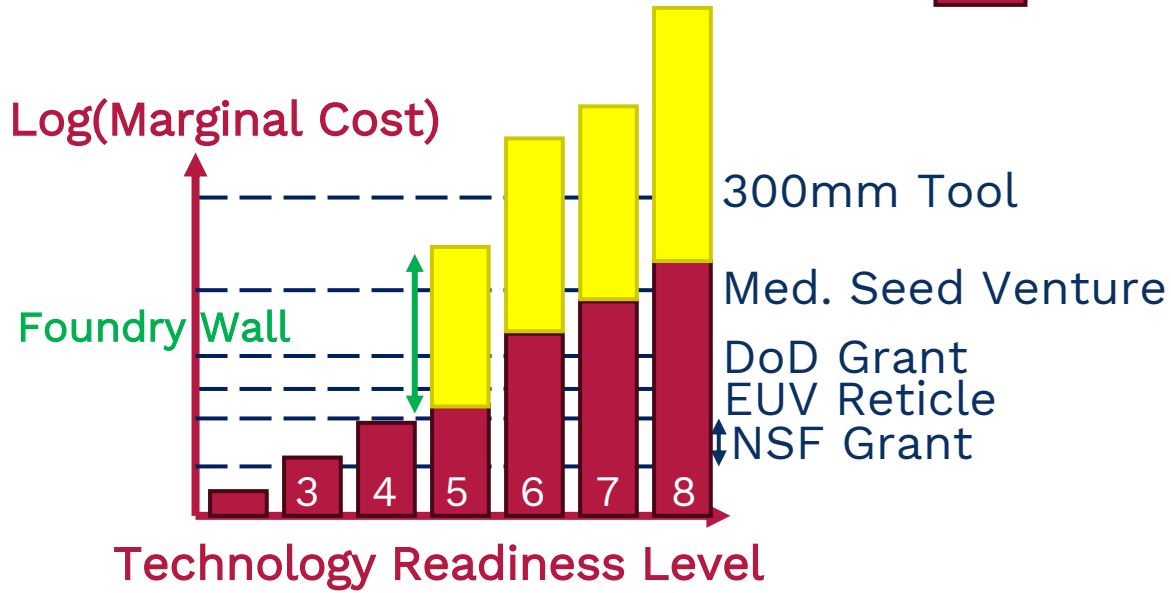
Technology Readiness Levels (TRL)



Stepping Stones Up the TRLs

 Marginal Costs

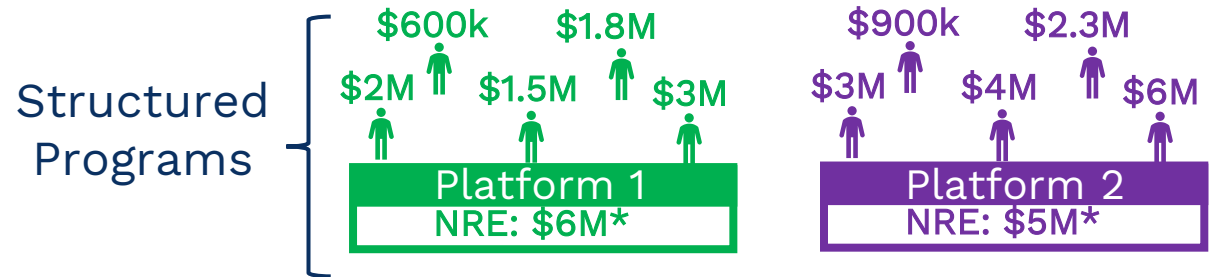
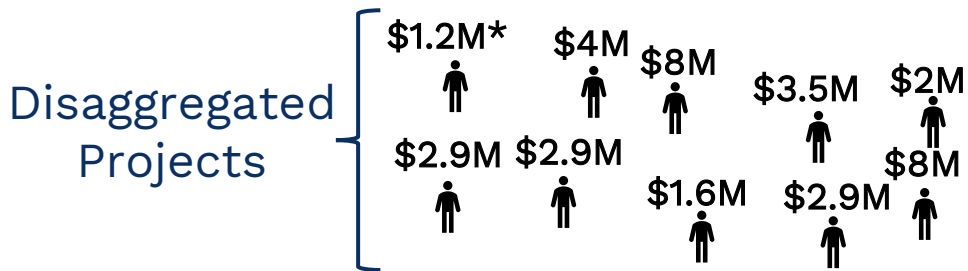
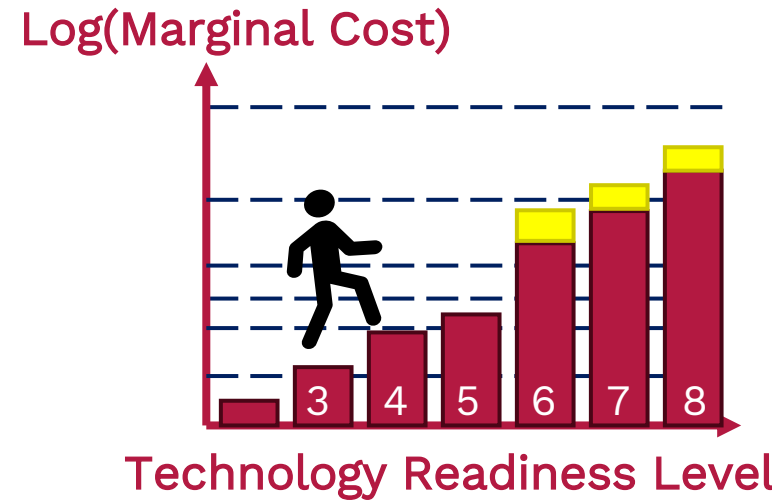
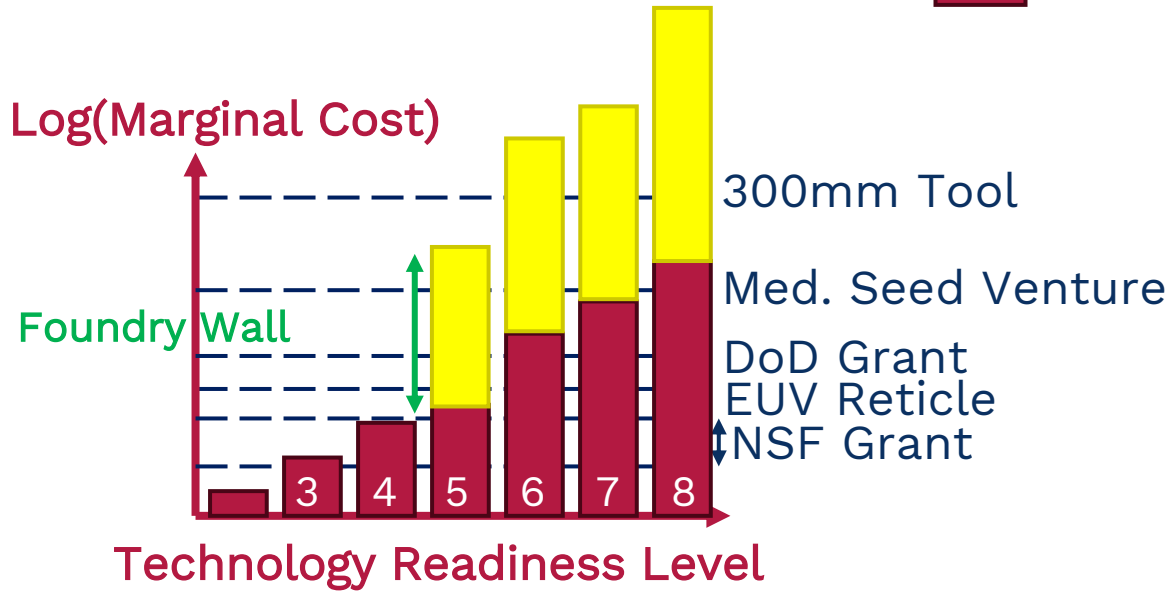
 NRE Foundry: EDA, Masks, Designs, Processes, validation



Stepping Stones Up the TRLs

 Marginal Costs

 NRE Foundry: EDA, Masks, Designs, Processes, validation



○ TVIP By the Numbers: 2-3-3-4-6

2 Program Tracks

3 Technology Focus Areas

3 TRL Bands

4 Major Deliverables

6 Tasks

○ TVIP By the Numbers: 2–3–3–4–6

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2 Anticipated Program Tracks



Generation Track

Proposed capabilities in relatively narrow areas

Completely new IP

End-to-end TRL spanning

Natcast own or access new mask set



Transition Track

Engagement to provide existing capability

Incremental redesign + new TRL levels

Can complete subset of program tasks

Can be outside of the 3 technology focus areas

Access to existing mask sets

○ TVIP By the Numbers: 2–3–3–4–6

2 Program Tracks

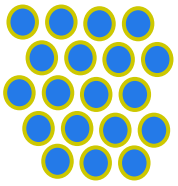
3 Technology Focus Areas

3 TRL Bands

4 Major Deliverables

6 Tasks

3 Technology Focus Areas for IP Generation



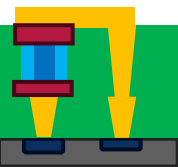
EUV Scale Logic or Mem Modules

Patterns/films to support basic process module development (ASD, Etch, CMP, etc.)



FEOL/MEOL Materials

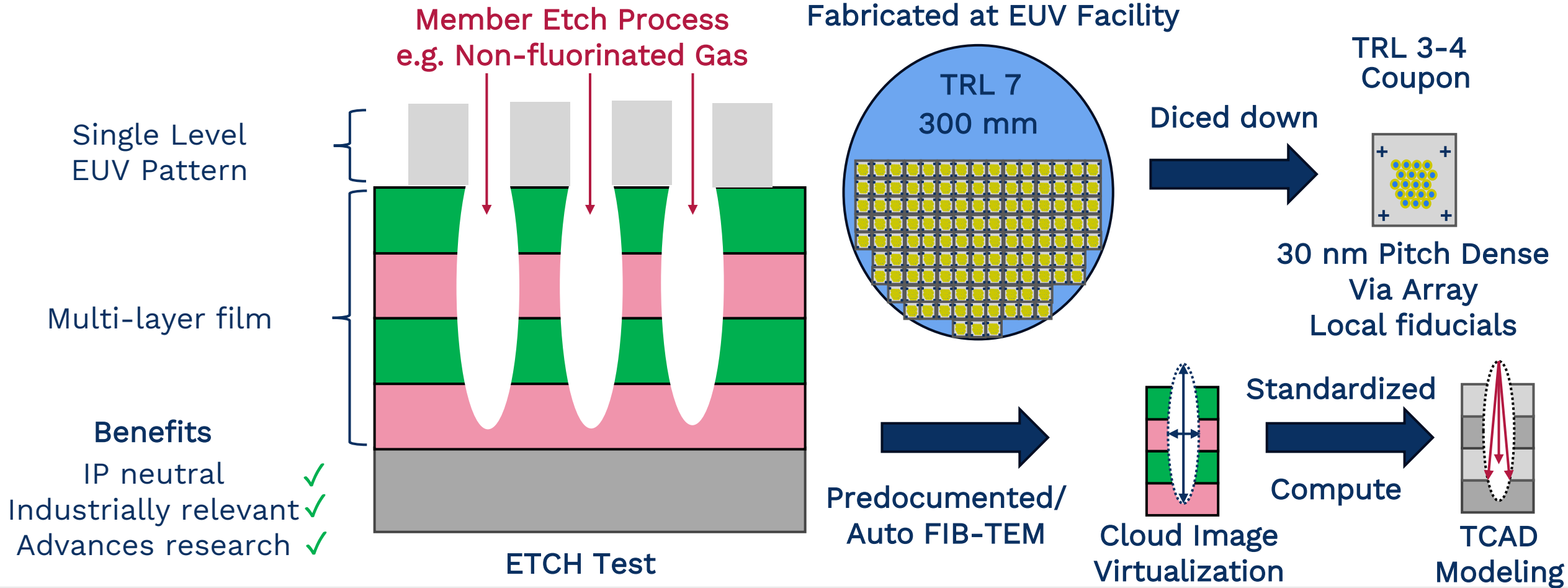
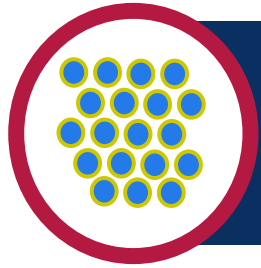
Exploring new gate stacks, contact materials, local interconnect, dielectrics, etc.



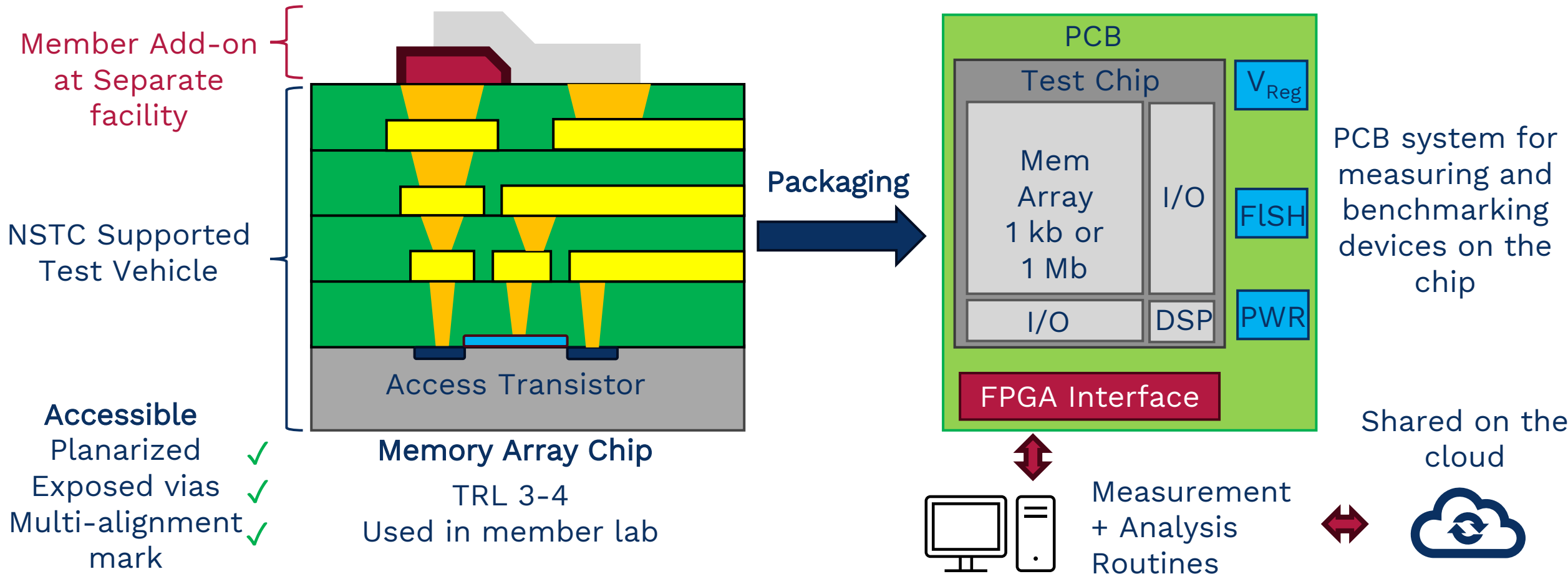
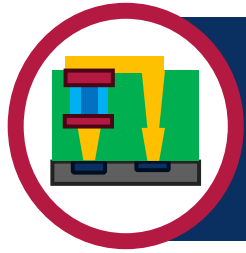
CMOS+X/BEOL Test Chips

Developing NVM devices, thin film transistors, 2D materials, interconnect, etc.

EUV Scale Example



CMOS+X Example



○ TVIP By the Numbers: 2–3–3–4–6

2 Program Tracks

3 Technology Focus Areas

3 TRL Bands

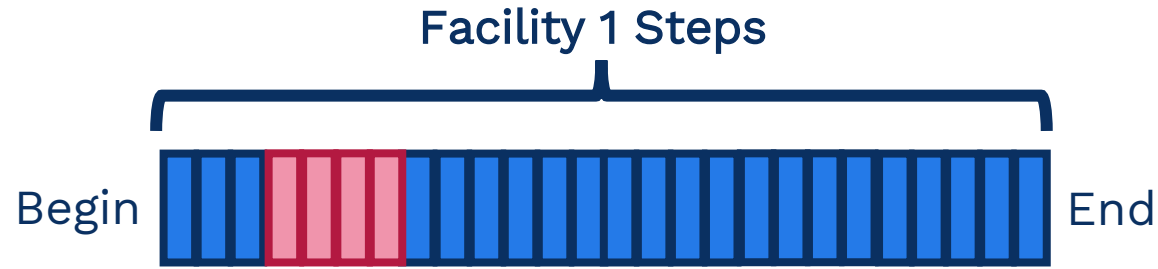
4 Major Deliverables

6 Tasks

3 TRL Bands and Prototyping Strategies*



TRL 7
Transition to Development:
Address fab compatibility



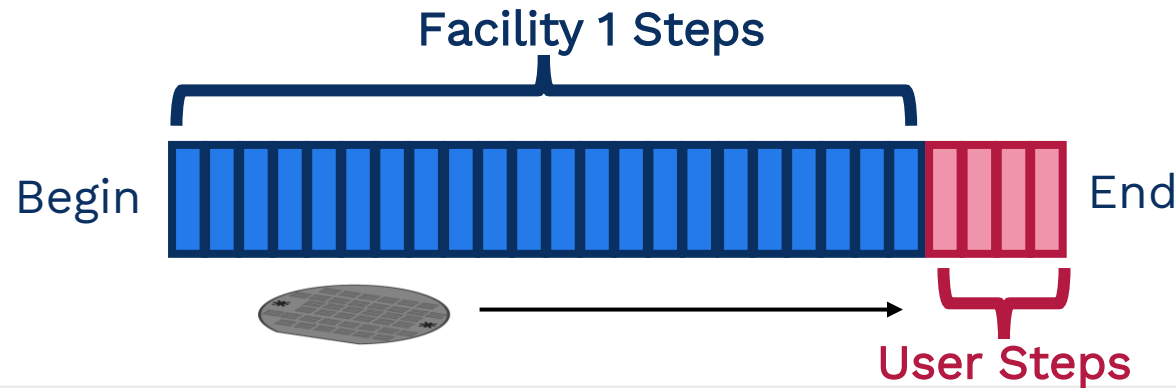
Earlier TRL work
enhances materials
compatibility studies

TRL 5-6
Assisted Prototyping
Establishing Viability



Wafer Coring to 100 mm
300 mm
Auto-stepper, scanner

TRL 3-4
Lab Finished Devices:
Enhancing basic research



Coupon Scale
Laser-writer
E-Beam
Minimal Processing

○ TVIP By the Numbers: 2–3–3–4–6

2 Program Tracks

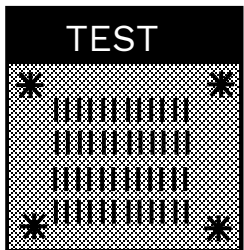
3 Technology Focus Areas

3 TRL Bands

4 Major Deliverables

6 Tasks

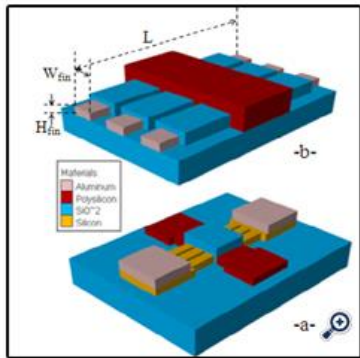
4 Anticipated Major Deliverables



Test Chip
Designs/Masks

Users
TRL 3-4 ✓
TRL 5-6 ✓
TRL 7 ✓

User Verification



Standardized
Measurement
and Analysis
Workflow

Key Docs
TV Manual
Material compatibility
assessment/criterion
Reference data
Transition plan
Curriculum

Documentation

○ TVIP By the Numbers: 2-3-3-4-6

2 Program Tracks

3 Technology Focus Areas

3 TRL Bands

4 Major Deliverables

6 Tasks

Anticipated Task Scope

Task 1: Refine and Review an Application's Requirements

- Deliver detailed technical requirements for **application within a Technology Focus area***
- Finalize plan for an interrelated solution for each of the **three TRL bands***:
 - TRL 3-4: Laboratory Research Environment
 - TRL 5-6: Relevant Research Environment
 - TRL 7: Industrial Research Environment

Additional Information

- Specifications reviewed by independent team in addition to program team
- Ensure best practices in multi-facility prototyping
- Confirm user base from basic research to the doorstep of development
- Produce a solution for each TRL band – from coupon scale to 300/200 mm
- **Go/No-Go** point

Anticipated Task Scope

Task 2: Design Test Vehicles and Tapeout

- Establish design capability at commercial foundry or advanced R&D facility
- Develop solutions spanning all TRL bands
 - May be a single mask set or multiple mask sets at multiple nodes
 - May require establishing a new reference process or multi-facility compatibility (e.g. new film stack, new 2nd facility process module, alignment marks, etc.)

Additional Information

- Address unique needs of various stakeholders
- Develop solutions enable establishing minimum viability of a new technology
- Develop test structures for materials compatibility and process health
- Designs to be reviewed before submission:
Go/No-Go

Anticipated Task Scope

Task 3: Establish a Measurement and Data Analysis Workflow

- Standardize the process of measurement
 - E.g. Pre-canned documentation, automatic FIB lamellae, electrical testing, etc.
- Standardize the process of analyzing data from standardized measurements
 - E.g. Basic statistical workflow, image recognition and extraction, TCAD integration through software API

Additional Information

- Post program, users should have little difficulty navigating data generation
- Standardizing measurements and data analysis enhances benchmarking
- Approaches geared to help create datasets

Anticipated Task Scope

Task 4: Deliver to Post-processing and Verification

- Teams should be prepared to verify that their Test Vehicle works for real applications
- TRL 3-4 and TRL 5-6 performers should demonstrate the use of the vehicle on a research application
- TRL 5-6 performers may create new Test Vehicle reference flow to finish wafers

Additional Information

- Post-processing teams should accurately reflect the potential user base
- Experiences using the test vehicle should be documented and best practices capture
- Data shared with NSTC

Anticipated Task Scope

Task 5: Develop Consortium Transition Plan

- Enable creation of repository of Test Vehicles for NSTC members
- Commitments to production and prospective cost of producing the vehicle, processes for NSTC to facilitate access
- Implementation of support of other CHIPS Programs
- Cloud deployment of data analysis and modeling tools for benchmarking and database building

Additional Information

- Consider the use of test vehicle after the program ends
- Test Vehicles which are more broadly accessible to the userbase will be preferentially supported
- Consider leading role as technology partners in future programs

Anticipated Task Scope

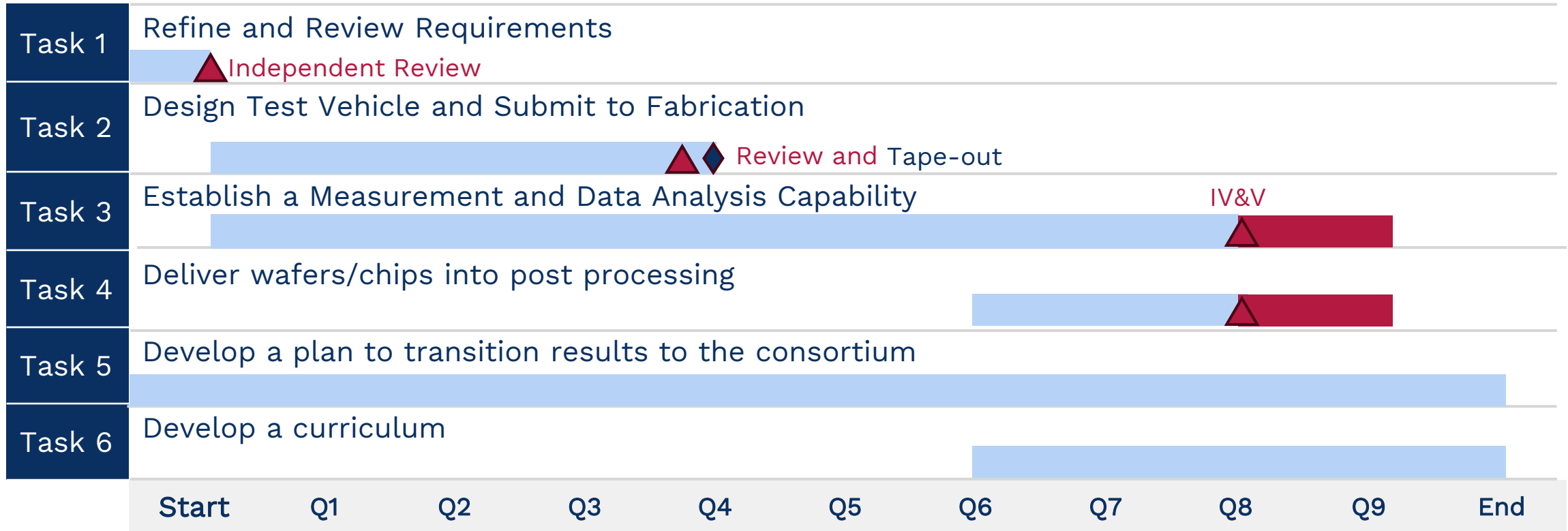
Task 6: Develop a Curriculum

- Identify learnings from the TVIP program most relevant to academic curriculum or a workforce training program
- Identify a suitable class or training program and develop a plan to integrate TVIP learnings into the training

Additional Information





- Integration of the TRL 3-4 test vehicles in fabrication courses is encouraged
- Enabling interrelated TCAD, modeling, or statistical analysis is encouraged

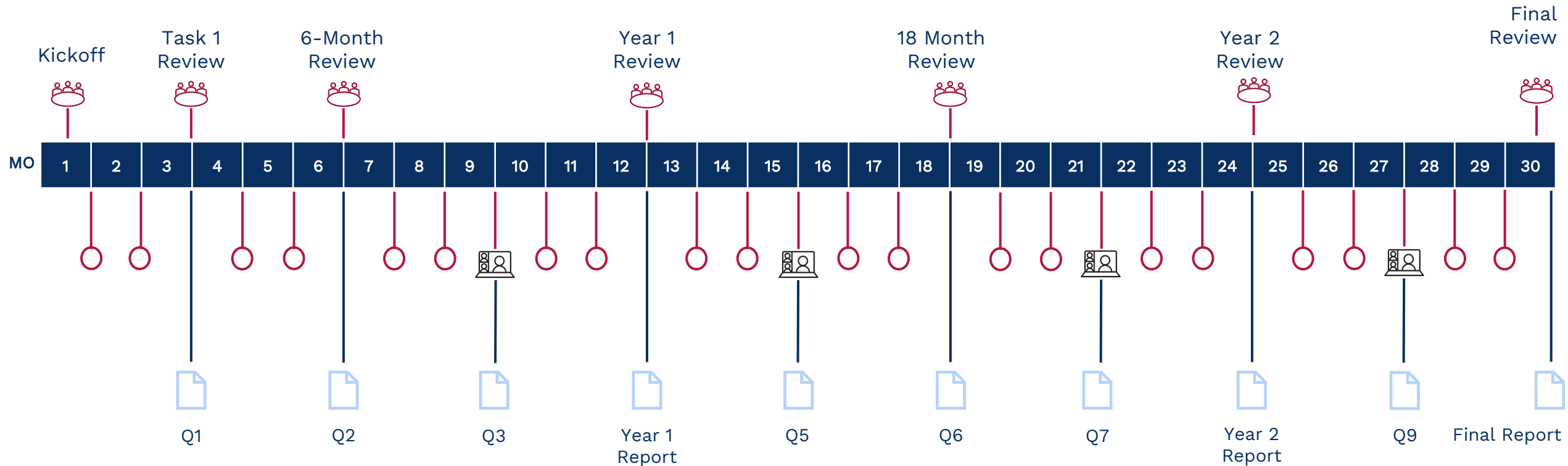
Sample Task Timeline for Single Test Vehicle*



*Timeline subject to specific TV requirements. *Faster is encouraged.*

TVIP Schedule

-  In-person Review
-  Virtual Status Meeting
-  Virtual PI Meeting
-  Report



Anticipated Evaluation Criteria: Priority Order

1. Utility and Benefits to NSTC Membership
2. Overall Scientific and Technical Merit
3. Relevance to Economic and National Security
4. Transition and Impact Strategy
5. Project Management
6. Cost Realism

TVIP Details and Key Dates

- **Anticipated Amounts:** Total program funding up to \$55M with 4-12 awardees anticipated.
- **Eligibility:** NSTC members at the time of award. Must be eligible to become NSTC members to propose.
- **Cost Sharing Requirements:** None
- **Teaming Opportunities:** Proposers' Day will facilitate teaming on Sept. 10, 2024. Teams encouraged to start discussions prior to this date. Engaging with TV potential users also encouraged!

Anticipated Key Dates

Call for Proposals Released	August 28, 2024
Proposers' Day	Sept. 10, 2024
Concept Papers Due	Sept. 16, 2024
Full Proposals Due	Oct. 21, 2024
Target Project Start	April 2025

NSTC Test Vehicle Repository

Natcast intends to create an accessible repository of mask sets and supporting workflows, documentation and datasets.

- IP and Data Rights required from Performers will be tailored to enabling a Test Vehicle repository for NSTC members after the program is over.
- Natcast will curate datasets related to Test Vehicle use during and after the Program ends and make these datasets available to NSTC members.

All proposers must identify:

- Pre-existing IP anticipated to be used to complete the project
- IP that may be developed with Natcast funding if awarded

Teaming

Teams could include any subset of:

- University researchers (R&D, training and workforce development)
- Semiconductor foundries and integrated device manufacturers
- Memory manufacturers
- Fabless semiconductor companies, including EDA/IP
- Startup companies
- U.S. government-funded labs

Vertically integrated teams across TRLs are strongly encouraged!

Fully Addressed at Proposers' Day

September 10, 2024 – The Westin Tysons Corner (Virtual Option)

- Fundamental research definition and implications
- Research security
- Commercial viability and domestic production
- Evaluation, selection criteria and review process
- Meeting and reporting schedule
- Budget format and payment terms

Registration to open this week. To reserve a room in the hotel room block, please book by Tuesday, August 27.

Proposers' Day – Sept. 10, 2024

Respond With Your Interest by Aug. 30

Panel Members and Moderators Needed

- Industrial Translation R&D barriers for new materials and device development
- Challenges of new materials/device introduction in fabrication facilities

Virtual Poster Session to Support Teaming

- Ample opportunities to share your work and research with others
- Breakout space and opportunities to plan collaboratively

Proposal Reviewer Pool Members

Facilities Interested in Supporting Test Vehicle Development

Please respond to Brian Hoskins at TVIP@natcast.org
[Natcast.org/research-and-development/TVIP](https://natcast.org/research-and-development/TVIP)

A Few Final Thoughts: Goals for After TVIP



Transition Track Programs Launched

NSTC members positioned to leverage existing IP for new programs
Multiple silicon proven designs revamped for new users across TRLs



Generation Track TVs Enabling Technology Transfer

New Test Vehicles spanning the 3 Technology Focus Areas and across the 3 TRL bands enabling benchmarking of research and the promotion of promising candidate technologies into advanced prototyping facilities.



A Thriving User and Member Community

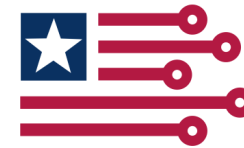
Users gain affordable access to new resources with clear pathways to advancing their research, guidelines for addressing material/process compatibility, and valuable datasets to enhance research programs

Thank You!



Sign up for our email
newsletter at Natcast.org

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