Scalable Memory Architecture Program (SMAP)
Call for Proposals (CFP)

Funding Opportunity Number: NAT-RD-25-0001

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Revision History

Date	Author	Change
April 14, 2025	Program Staff	Version 1.0

National Semiconductor Technology Center (NSTC)
Call for Proposals
Executed by Natcast, the operator of the NSTC
Scalable Memory Architecture Program (SMAP)
Executive Summary

Funding Opportunity Title: Scalable Memory Architecture Program (SMAP)

Funding Opportunity Number: NAT-RD-25-0001

Dates: Key dates are given below. *All submissions are due by 5:00 pm EDT on the specified dates.*

Activity/Event	**Date**
SMAP CFP Released	04/14/2025
SMAP Proposers' Day	04/29/2025
Concept Papers Due	05/06/2025
Question Submission Deadline	05/13/2025
Full Proposals Due	**06/17/2025**
Target Project Start	Dec-2025

Concise Description of Funding Opportunity: SMAP (pronounced ess-map) aims to address the growing disparity between processor speed and memory bandwidth (also known as "the memory wall challenge") by developing scalable, workload-driven architectural solutions that leverage new memory technologies and advanced packaging techniques. This program aims to provide NSTC members with the data, tools, and technology assessment capabilities needed to optimize performance, reduce latency, and improve energy efficiency in high computing data center systems and energy constrained edge systems. By focusing on new memory technologies, advanced packaging, and programmability, this program seeks to foster innovation and maintain a competitive edge in the rapidly advancing semiconductor industry.

Anticipated Amounts: Total program award funding up to $33.5M with 8-14 awards is anticipated. Individual awards are expected to range from $2-$5M.

Eligibility: Proposers and funded participants must be eligible to become NSTC members to submit proposals. If selected for the award, proposers and funded participants must become NSTC members (https://natcast.org/nstcmembership) in order to receive the award. Eligible proposers include domestic for-profit organizations, non-profit organizations, and institutions of higher education. See Section 3 for additional details on eligibility.

Concept Paper: Proposers must submit a concept paper prior to submitting a full proposal. Proposers can submit concept papers for one or both **Focus Areas** of the SMAP program. Each concept paper should be limited to 3 pages with separate submissions required for each **Focus Area**.

Proposers will receive feedback within 14 days after the closing date. All concept paper submitters may proceed to full proposal submission regardless of feedback.

A concept paper template is provided separately at https://natcast.org/research-and-development/smap while submission guidelines and requirements are presented in Appendix B. Cover pages, references, and glossaries are not included in the page count, though figures and tables are counted. Proposers should follow the formatting guidelines in Section 7.2.1 and reference the template for complete submission requirements, including technical approach, preliminary work, planned achievements, and estimated budget information.

The composition of the team can change between concept paper submission and full proposal submission. Concept papers will be evaluated against the first two criteria laid out in Section 5.1: Evaluation Criteria. Concept papers may be submitted directly by any individual who is authorized to agree to the submission terms and conditions on behalf of the submitting organization(s).

Proposal Submissions: Proposers are encouraged to submit proposals for at least one **Focus Area** and must address all the **Technology Areas** and tasks. Separate proposals must be submitted for each **Focus Area** if proposing work in both data center compute systems and edge compute systems. A Proposal template is provided separately at https://natcast.org/research-and-

development/smap while submission guidelines and requirements are presented in Section 4.0 and Appendix B, respectively.

Teaming Opportunities:

Proposers are encouraged to form partnerships for expertise across **Focus Areas** and **Technology Areas** with other organizations, although such partnerships are not required for proposal submission. Please refer to Appendix C.7 *Proposed International Collaborations* for guidance about foreign facilities and collaborators.

To facilitate teaming arrangements, attendees at the proposer's day events will have the opportunity to indicate their interest in collaboration. After registration for these events, participants can specify their teaming availability and interests, allowing potential partners to identify appropriate collaboration opportunities.

Contract Type: Firm-fixed price with milestone payments with predefined deliverables.

Cost Sharing Requirements: None

Website and Frequently Asked Questions (FAQs): https://natcast.org/research-and-development/smap

Overview of Natcast's competition and awards policy:

https://natcast.org/research-and-development

Contact Information: For questions regarding the Program, Award Management, or Technical Assistance with Proposal Submission, please email: smap@natcast.org

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1.0 Funding Opportunity Description

1.1 Introduction

The National Semiconductor Technology Center (NSTC) was established pursuant to the CHIPS Act as a public-private consortium dedicated to semiconductor research and development (R&D) in the United States (U.S.). The NSTC convenes the U.S. government, allied and partner nations, and organizations across the semiconductor ecosystem—including academia and businesses of all kinds—to address the most challenging barriers to continued technological progress in the domestic semiconductor industry, including the need for a capable workforce. The NSTC reflects a once-in-a-generation opportunity for the U.S. to drive the pace of innovation, set standards, and re-establish global leadership in semiconductor design and manufacturing. The mission of the NSTC is to serve as the focal point for research and engineering throughout the semiconductor ecosystem, enabling disruptive innovation to provide U.S. leadership in the industries of the future. Natcast is a purpose-built, non-profit entity designated to operate the National Semiconductor Technology Center (NSTC) by the Department of Commerce.

The NSTC is mandated with three goals and executes the programs towards achieving those goals through combination of new capabilities along with affiliated and collaborative relationships with existing entities. The NSTC goals, as per NSTC Vision and Strategy document [1], are identified as: (1) Extend U.S. leadership in foundational technologies for future applications and industries and strengthen the U.S. semiconductor manufacturing ecosystem, (2) Reduce significantly the time and cost to prototype innovative ideas for member organizations and (3) Build and sustain a semiconductor workforce development ecosystem. This effort will require research and collaboration from stakeholders across the semiconductor supply chain, including industry experts, academic proposers, national laboratories, start-ups, government agencies, and others within the community.

The Scalable Memory Architecture Program (SMAP) is a 30-month initiative aimed at addressing the growing disparity between processor speed and memory bandwidth, commonly known as the "memory wall" [2]. This program will fund projects to develop scalable, workload-driven architectural solutions that leverage new memory technologies and advanced packaging techniques. The goal is to optimize performance, reduce latency, and improve energy efficiency in high computing data center systems and energy-constrained edge systems. At a minimum, the solutions should be able to integrate new memory technologies, manage memory efficiently, utilize innovative

packaging techniques, and focus on programmability to meet the demands of diverse computational environments.

High-performance computing systems are increasingly reliant on System on Chips (SoCs) comprised of specialized compute accelerators (e.g., GPUs, TPUs, FPGAs) working alongside CPUs in a heterogeneous compute system to handle massive workloads efficiently. However, despite their high computational performance, these systems are currently challenged by the limitations of the memory wall [2], [3], [4]. This occurs due to the growing disparity between the rate at which data can be processed and the slower speed at which data can be moved within the system. Modern computing systems are predominantly processor-centric, designed to move data to computation, which exacerbates several key trends in computing that create performance, scalability and energy bottlenecks.

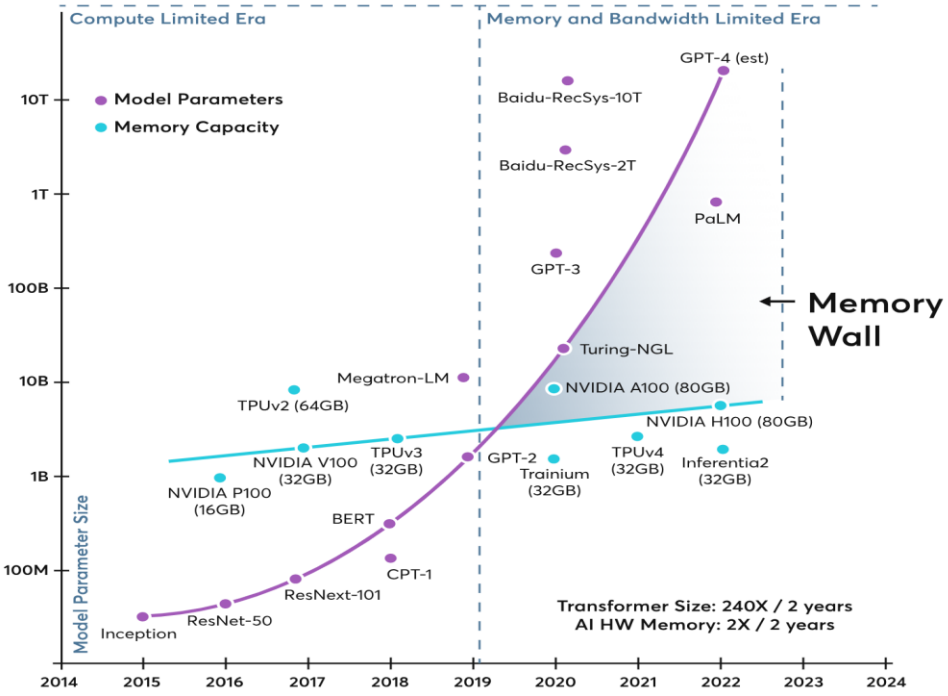

Figure 1. *Description of Memory Wall (Courtesy Ayar Labs).*

This trend causes memory wall problems with the following characteristics:

1. Many important applications (e.g., machine learning, genome analytics, databases, graph analytics, high-performance computing, mobile, and server-class workloads) are increasingly data-intensive. As workloads increase in size (e.g., deep learning models), the demand for memory bandwidth grows, pushing

the limits of traditional memory devices (such as SRAM and DRAM) in terms of throughput, capacity, reliability, and energy consumption.

2. Energy consumption is a critical limiting factor in almost all computing platforms. Moving data, on-chip and from off-chip, is much more expensive in terms of energy, latency, and bandwidth compared to computation. As computation becomes more heterogeneous and distributed, the movement of data between different memory regions, hierarchies, and computing units becomes a significant overhead, leading to degraded performance and higher overall costs.

These impacts are acutely felt in the high computing data center systems and energy constrained edge systems of today [4], [5].

1.2 Motivation

In recent years, technology trends have shown significant advancements in computational capabilities, particularly with the development of specialized processing units such as CPUs, GPUs, and NPUs. However, over the past 20 years, the scaling of compute, memory, and interconnect technologies have revealed a disparity: peak server hardware FLOPS has been scaling at 3.0×/2yrs, outpacing the growth of DRAM and interconnect bandwidth, which have only scaled at 1.6 and 1.4 times every 2 years, respectively. This disparity has made memory and data movement, rather than compute, the primary bottlenecks in AI applications [6].

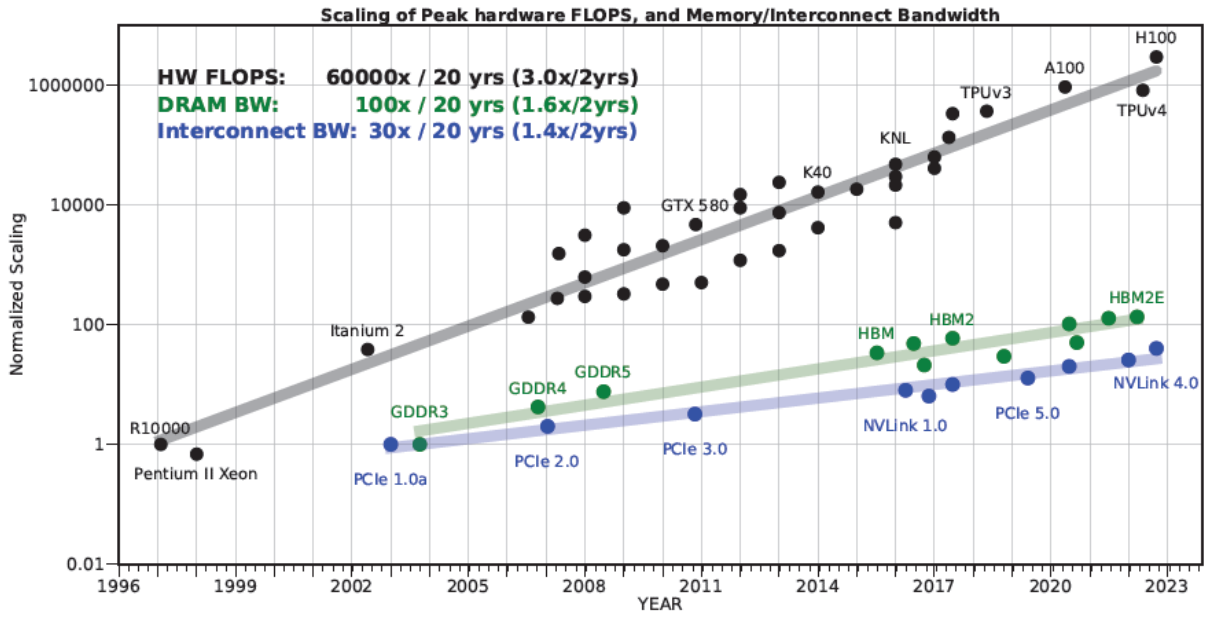

Figure 2. *Scaling of Compute, Memory and Interconnect Technology (Courtesy [5]).*

Despite remarkable progress in developing specialized processing units optimized for various computational tasks (e.g. CPU, GPU, NPU etc.,), there has been a comparative lack of advancement in harnessing new memory technologies to address the same workload-specific optimizations [3].

As applications continue to become more data-intensive, processor-centric systems will increasingly spend more energy towards data movement leading to degraded performance and increased overall cost. At the same time, conventional memory technology is facing many technology scaling challenges in terms of robustness, energy, and performance.

Emergence of custom accelerators shows promise of significant performance improvements for the workload, though many encounter programming challenges that limit their broader adoption in the industry [2]. The increased number of cores and parallel units on processing systems adds complexity, necessitating careful scheduling and load balancing to avoid inefficient data movement. Additionally, heterogeneous and distributed computing introduces data coherency bottlenecks, where maintaining data coherency incurs additional energy costs, even though it simplifies programming.

The incorporation of new memory devices and advanced packaging technologies is crucial for addressing the memory wall challenge. Integration of new memory devices with the properties that are optimized for workloads along with traditional memories are expected to bring significant performance boosts and energy efficiency. Advanced packaging technologies enable assembly of disparate (e.g.: logic/memory components of difference process nodes) components in a system-in-package to deliver higher performance which was not possible with monolithic designs.

The impact of technology scaling is assessed at the block level through DTCO (design-technology Co-optimization) methodology, synergizing design and process technology to enhance performance, power efficiency, and cost-effectiveness. On the other hand, current system design research is primarily based on new architectures for a target application and design constraints, largely abstracting the impact of underlying technologies. As technology scaling stagnates, improving system performance faces several bottlenecks—memory, power, and bandwidth walls. STCO (system-technology co-optimization) is a promising paradigm for leveraging the synergy between emerging technology and workload driven system architectures to achieve higher efficiency and performance.

The SMAP Program is motivated by the critical need to address the memory wall, which significantly impacts the performance and energy efficiency of high computing data

center systems and energy-constrained edge systems. The program aims to develop scalable, workload-driven architectural solutions by employing STCO methodologies to evaluate new technologies in the context of system design. By integrating new memory technologies (beyond SRAM, DRAM and flash), memory management techniques, advanced 2.5D/3D packaging technologies, and focusing on programmability, the program seeks to optimize system performance and energy efficiency for industry-relevant workloads.

SMAP aims to foster innovation in the rapidly advancing semiconductor industry. By funding multiple research teams to conduct architectural studies on new memory devices, advance architectures, and advanced packaging technologies tailored to industry-relevant workloads, the program aims to yield practical solutions for real-world applications. These solutions will help address the memory wall challenge, improve system speed, reduce energy consumption, and enhance computational capabilities across diverse computational environments.

Natcast will support multiple research teams to conduct architectural studies for new memory technologies for various industry-relevant workloads. These studies will quantify the extent to which new memory architectures can address the memory wall challenge. Each research team will be required to:

- Develop and test new architectural models that integrate new memory devices and advanced packaging technologies.
- Quantify performance improvements, focusing on metrics such as latency, bandwidth, power efficiency, and scalability.
- Perform trade-space analysis across the new memory device and advanced packaging technology features in the context of system workloads.

Provide detailed reports and data that can be used to compare different approaches and identify the most promising solutions.

1.3 Goals and Outcomes

The overarching goal of SMAP Program is to provide NSTC members with data, tools, and technology assessment capabilities to form customized, multi-pronged approaches to the memory wall challenge. Due to the inherent challenges associated with diverse workloads and evolving memory technologies, the SMAP Program aims to produce comprehensive architectural studies, advanced simulation tools, detailed datasets and trade-space reports around new memory and advanced packaging technologies tailored

to members' specific application requirements. The community assets generated through the SMAP Program include these architectural studies, performance models and tools, which serve as essential resources for evaluating and implementing new memory architectures. By leveraging these resources, NSTC members will be able to explore and implement novel memory architectures, optimize performance, reduce latency, and improve energy efficiency in their systems. This comprehensive approach is designed to address NSTC members' unique demands of their applications, fostering innovation in the rapidly advancing semiconductor industry.

High level program elements of SMAP are described below. SMAP program scope and structure are described in section 1.4. SMAP intends to study a wide variety of industry relevant workloads (such as AI/ML training, AI inference, data analytics, transactional databases, knowledge extraction, and search). However, to better define the focus of SMAP, we have limited the architecture studies to two **Focus Areas:** (1) data center compute systems and (2) edge compute systems, with the goal that the program results and collaterals developed would be extensible to other compute systems.

The study performed under the SMAP Program will comprehensively cover three **Technology Areas:**

1. **New Memory Devices**
   Integrating new memory devices with traditional memories like SRAM, DRAM and Flash are expected to bring significant performance boosts and energy efficiency[4]. Research programs that focus on new memory device technologies that are TRL 3 and above will be considered. A few new memory devices with specific attributes are listed below, but others not listed will also be considered within the scope.
   - **Spin-Transfer Torque MRAM (STT-MRAM):** Known for its non-volatility and high endurance, STT-MRAM can significantly improve data retention and power efficiency.
   - **Phase-Change Memory (PCM):** PCM offers high storage density and fast read/write speeds.
   - **Resistive RAM (RRAM):** RRAM is characterized by its low power consumption and high scalability.
   - **Gain Cell Memory:** This type of memory offers a balance between speed and density.
   - **Ferroelectric RAM (FeRAM) and Ferroelectric Field-Effect Transistors (FeFET):** These technologies combine non-volatility with high-speed operations.

2. **Advanced Packaging Technologies**

   Advanced 2.5D and 3D packaging technologies [7] will enhance memory performance by enabling higher memory bandwidth, reduced latency, and better power efficiency through closer integration of memory and processing units. Research programs that focus on advanced packaging technologies that are TRL 3 and above will be considered.

   - **2.5D Packaging:** Two or more active semiconductor dies are placed side-by-side on an interposer to achieve extremely high die-to-die interconnect density. 2.5D offers a good balance between cost and performance compared to 3D packaging.
     - **Interposers:** Usage of interposers of any material to connect semiconductor dies that allow integration of heterogeneous components with different pitch, size, material, and process nodes.
     - **Silicon Bridges:** Localized Si bridges to strategically utilize silicon where fine features are essential, addressing area constraints of full Si interposers.
     - **TSVs and HDI:** high-density interconnects (HDI) to connect the silicon dies and Through-Silicon Vias (TSVs) to connect the silicon die to interposer offering high density and low latency.
   - **3D Packaging:** 3D packaging technologies in semiconductors refer to advanced packaging techniques that involve stacking multiple silicon dies or chiplets vertically to create a compact, high-performance system. This vertical stacking of chips is used to improve the functionality and performance of semiconductor devices by reducing the footprint and interconnect distances, offering greater integration, and higher performance.
     - **3D packaging types:** Several 3D packaging types exist with varying cost, complexity profile as per industry needs - TSV-based 3D ICs, Wafer-Level Packaging (WLP) + 3D, Chip-on-Chip (CoC), Chip-on-Wafer (CoW) + 3D. Package-on-Package (PoP)
     - **Through-Silicon Vias (TSVs)**: Vertical electrical connections that pass through a silicon wafer or die, enabling communication between stacked chips.
     - **Die Stacking:** Multiple dies are stacked vertically, improving performance and integration.
     - **Microbump Technology**: Based on thermal compression bonding (TCB), it's used for interconnections between stacked dies.

- **Hybrid Bonding**: Advanced technique allowing for ultra-fine interconnect pitches in the single-digit micrometer range.

3. **Programming Model**
   Programmability will be considered a critical component of new memory architecture investigations and definitions to increase the chance for industry adoption.
   - Develop new data types and programming constructs that allow workload data mapping to new memory devices.
   - Explore methods to extend the current programming languages and compiler for the new programming constructs.

The SMAP program will have the following activities.

- **Technology investigations**
  - Examine new memory technologies that could provide significant improvements in current architectures. Memory technologies that will be eligible for the SMAP Program may include, but are not limited to, STT-MRAM, PCM, RRAM, Gain Cell, FeRAM, and FeFET. Assess through modeling and simulation the impact of new memory technologies on overall system performance and their potential for integration into future architectures.
  - Investigate through modeling and simulation the potential of advanced 2.5D, 3D packaging techniques to address the memory wall limitations. Explore how 2.5D, 3D integration can enhance memory performance, reduce latency, and improve bandwidth.

- **Tailoring Solutions to Industry-Relevant Workloads:**
  Solutions developed should be tailored to industry-relevant workloads to ensure their practical applicability. This involves:

  - **Workload Profiling:** Conducting detailed profiling of target workloads such as AI/ML training and inference, big data analytics, transactional databases, and real-time data processing.
  - **Customizing Architectures:** Designing memory architectures that are optimized for the unique demands of these workloads. For instance, AI/ML workloads may benefit from memory technologies that offer high bandwidth and low latency, while big data analytics might require solutions that provide high storage density and energy efficiency.
  - **Performance Evaluation:** Solutions should use industry-standard benchmarks to evaluate the performance of new architectures against

current solutions to ensure that they meet or exceed the required performance standards.

- **Example Workloads:**
  - **AI/ML Workloads:** These workloads may benefit from memory technologies that offer high bandwidth and low latency, enabling faster training and inference.
  - **Big Data Analytics:** Solutions that provide high storage density and energy efficiency are crucial for handling large datasets and performing complex analytics.
  - **Transactional Databases:** Memory architectures that ensure data integrity, low latency, and high endurance are essential for transactional database applications.
  - **Real-Time Data Processing:** Solutions that offer ultra-low latency and high-speed data access are critical for real-time processing applications.

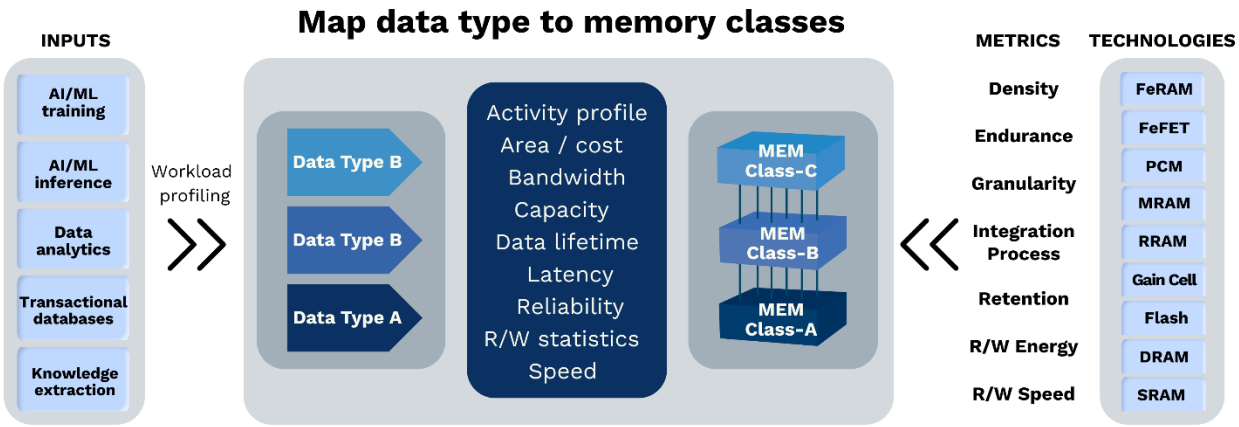

Figure 3. *Mapping by abstracting data types from software applications and memory devices. Adapted from [4].*

- **Trade-Space Analysis:**
  Solutions should include trade-space analysis to evaluate sensitivities of technology attributes in the context of system workload performance to develop recommendations on the promising solutions.
  - Perform comprehensive trade-space analysis on new memory technology features such as power, energy, retention time (from microseconds to several seconds), capacity, fine-grained sub-array, silicon core transistor redesign

(process complexity), number of memory layers, endurance, read/write speed, and bandwidth.

- Perform comprehensive trade-space analysis on advanced packaging technology features such as packaging types, materials, interconnects (TSV, HDI, Microbump and hybrid bonding), yield and cost.

To maintain focus and ensure meaningful progress in this initial program, certain approaches will be deemed out of scope. Specifically, architectural concepts or optimizations that do not include the integration of new memory devices and advanced packaging technologies will not be considered. Additionally, the focus of this CFP is limited to single system-on-chip (SoC) or system-in-package (SiP) and does not include multi-chip scale-out solutions. Accordingly, chip-to-chip (or SoC to SoC) interconnects are out of scope. When providing feedback to concept papers, Natcast may deem other approaches out of scope.

Key Deliverables

- Abstract Layer Modeling Tools**:** Tools for performing analysis and efficacy studies at an abstract layer to understand the potential benefits and trade-offs of different architectural approaches.
- Memory Device Modeling and Benchmarking Tools: Tools for modeling and benchmarking various memory devices.
- Programming Constructs and Languages: New data types that can be mapped to suitable memory devices and address challenges towards programming for new architectures.
- Reports: Comprehensive documentation of baseline and proposed architectures, performance results, trade-space analysis, benchmarks, programming models, and tools for new memory and advanced packaging technologies, with iterative updates to reflect ongoing findings.

Program Outcome

The program integrates multiple layers of the system stack to address the memory wall challenge and foster a cohesive approach to enhancing system performance. By breaking down silos between architectural techniques and device technology development, the program encourages interdisciplinary collaboration and innovation. It introduces new paradigms for memory technology mapping and development that are tailored to specific workload characteristics for optimal performance and energy efficiency. By synergizing hardware and software considerations, the program aims to remove barriers to industry adoption, ensure practical and effective implementation of

new technologies. The program outputs are expected to be applicable to a wide range of stakeholders, including logic and memory companies, system companies, and fabless semiconductor firms, thereby promoting widespread industry innovation. Additionally, the program outputs would provide directions to Natcast to undertake prioritized initiatives via hardware prototypes ensuring that research findings are practically implemented and drive continued progress in the semiconductor industry.

1.4 Scope

The SMAP program aims to use a multifaceted approach to overcome the memory wall challenge. Proposers are encouraged to submit proposals for at least one **Focus Area** (i.e., datacenter compute system or edge compute systems). If proposing to work in both, separate proposals must be submitted for each **Focus Area**. Each proposal must cover all three **Technology Areas**.

The program is designed into three phases as outlined below.

Phase 1: Baseline

This phase establishes the reference hardware architecture and workloads relevant to **Focus Area** that is constrained by memory wall bottleneck. Performance results can often be difficult to interpret when there are numerous variables or assumptions. To reduce these complexities, this phase will focus on conducting the baseline study and meticulously documenting the data that will be used in later phases. Proposers are encouraged to use publicly available processor architectures as the baseline. The base hardware architecture should only include technologies that are demonstrated to be at Technical Readiness Level (TRL) of 6 and above.

While SMAP intends to cover the study of a wide variety of industry relevant workloads (such as AI/ML training, AI inference, data analytics, transactional databases, knowledge extraction, and search), there is a preference to select more proposals focusing on AI/ML training and inference workloads due to well demonstrated memory wall impact. Proposers are encouraged to use publicly available AI models, datasets and benchmarks for the analysis (for e.g. MLPerf [8])

Task 1: Detailed Requirements Development

- Establish baseline architecture, workloads, benchmarks, and key performance metrics [6] for the chosen **Focus Area**. Document the base architecture assumptions, including logic, memory, process, frequency, bandwidth, capacity,

and other relevant factors. Natcast may provide feedback on the plan for normalization across all research teams.

- Identify new memory and advanced packaging technologies that will be used in the study. Document the key performance attributes of the new memory devices, such as read/write latency, energy consumption, capacity, and persistency. Also, identify the key performance attributes of the packaging technologies, such as interconnect bandwidth, die/chiplet area, and process node. Given that the physical packaging aspects (such as power delivery, routing, thermal etc.) are unknown, reasonable estimates should be used and documented.
- Identify the performance modeling framework, tools, and programming languages that will be used to develop the models. Proposers are encouraged to use or extend publicly available Design Space Exploration (DSE) tools such as ZigZag, TimeLoop, Maestro [9], [10], [11].

Task 2: Baseline Architecture Performance Study

- Develop tools to derive test vectors from the selected workloads.
- Develop performance model for baseline architecture. The modeling framework should be developed to be easily configurable and extendable for various architecture elements such as compute, memory, fabric, bandwidth, latency, and capacity.
- Derive key performance metrics and benchmarks of baseline architecture's performance for the selected workloads. This data will serve as the project's baseline, enabling the quantification of improvements in subsequent phases.

Deliverables:

- Baseline Architecture report - Report that describes the baseline architecture of the chosen **Focus Area**. The report should detail the methodology used to select the architecture, workloads and methods to derive the workload input data for the performance models. Additionally, it should outline the benchmarks and the key performance metrics that will be studied. The report should also include information on new memory technologies along with key performance attributes, as well as the advanced packaging technologies and the assumptions made.
- Baseline Performance report – Report should present the results from the architecture study. It should include the key performance data derived from the performance model, along with commentary on workload characteristics and performance limitations due to memory wall bottlenecks. The report should describe the plan for the trade-space analysis along the key vectors, including

the delivery of the performance models, input and output data, and tools/scripts used for the analysis.

Phase 2: Investigate

Propose novel architectures that make use of the new memory devices and advanced packaging technologies for the selected **Focus Area**. Perform architecture studies described in **Task 3 - Integration of New Memory Devices** and/or **Task 4 - Integration of Advanced Packaging Technologies.** These tasks can be completed in any order, but trade-space analysis in **Phase 3** should include both aspects. The program's intent is to deliver performance and trade-space analysis reports for each task independently during this phase, before releasing combined reports in **Phase 3.**

Task 3: Integration of New Memory Devices

The proposal should include any new memory device technologies that are demonstrated to be at Technical Readiness Level (TRL) of 3 and above for the study.

3.1: Data mapping and Workload Profiling

- Map data to memory classes through detailed workload profiling for the selected workloads.
- Evaluate memory attributes such as capacity, data lifetime, read/write statistics, activity profile, latency, bandwidth, power, speed, area/cost, and reliability.
- Develop abstract layer modeling tools for performance analysis and efficacy. Create tools for modeling and benchmarking memory devices.

3.2: Architecture Studies – New Memory Devices

- Investigate novel system architectures while using the data mapping in task 3.1 to improve overall energy efficiency thus overcoming the memory wall challenge while maintaining the other metrics relevant to the workload.
- Identify necessary improvements of each memory technology to be effectively utilized in software use cases, grounding these improvements on state-of-the-art macro demonstrations.
- Evaluate programming aspects for novel architectures and investigate, develop new data types, programming constructs that allow workload data mapping to new memory devices. Explore methods to extend the current programming languages and compiler for the new constructs.
- Demonstrate performance gains and energy efficiency over the Baseline performance from Phase 1.

3.3: Trade-Space Analysis – New Memory Devices

- Perform comprehensive trade-space analysis considering factors such as power, energy, retention time (from microseconds to several seconds), capacity, fine-grained sub-array, silicon core transistor redesign (process complexity), number of memory layers, endurance, read/write speed, and bandwidth.

Deliverables:

- Task 3 Architecture report – Report that describes the proposed architecture with new memory devices used. It should detail the methodology used to map the workload data to memory classes and impact on the performance. The report should also describe the benchmarks and the key performance metrics that are studied.
- Task 3 Performance report – Report containing the results from the architecture study, including comparisons with the baseline. The report should include updated benchmarks, metrics and charts demonstrating improvement over Phase1 Baseline data via state-of-the-art macro demonstrations. The report should include trade-space analysis results and recommendations on the promising solutions and challenges in adopting new memory technologies.
- Task 3 Programming Model report – Report on programmability for the architecture along with delivery of macros, languages and compiler created.
- Task 3 Performance Models and Tools – Updated Performance modeling framework, abstract layer modeling tools, and memory device modeling and benchmarking tools.

Task 4: Integration of Advanced Packaging Technologies

The Proposal should include any Advanced Packaging Technologies that are demonstrated to be at Technical Readiness Level (TRL) of 3 and above for the study.

4.1: Create Advanced Packaging Profiling System

- Extend the architecture defined in Phase 1 by incorporating advanced packaging technology attributes such as processing throughput, improved bandwidth, capacity and reduced energy, and latencies. Reasonable assumptions should be made with respect to overheads associated with fabric, package routing, power delivery and thermal management, while keeping the compute logic and area aspects normalized to the baseline architecture defined in Phase 1.
- Develop abstract layer modeling tools for performance analysis and efficacy. Create tools for modeling and benchmarking advanced packaging features.

4.2: Architecture Studies – Advanced Packaging

- Investigate novel system architectures using advanced packaging technologies to achieve significant improvements in memory wall performance. Focus on enhancing overall energy efficiency while simultaneously maintaining other key metrics relevant to the workload. Specific attention to be paid to fabric challenges to move data from different components, chiplets and dies connected through advanced packaging technologies.
- Identify necessary improvements of advanced packaging feature to be effectively utilized in software use cases, grounding these improvements via performance modeling simulations.

4.3: Trade-Space Analysis – Advanced Packaging

- Perform comprehensive trade-space analysis considering factors such as performance, power consumption, scalability, reliability, size, and form factor, along with packaging technologies such as packaging types, materials, interconnects (TSV, HDI, Microbump and hybrid bonding)

Deliverables:

- Task 4 Architecture report – Report that describes the proposed architecture with the advanced packaging technologies used. It should detail the methodology used to map advanced packaging techniques that are relevant to improved performance. The report should also describe the benchmarks and the key performance metrics that are studied.
- Task 4 Performance report – Report containing the results from the architecture study, including comparison over Task 3 report. The report should also include updated benchmarks, metrics and charts demonstrating improvement over Task 3 data via performance modeling simulations. The report should include trade-space analysis results and recommendations on the promising solutions and challenges in adopting advanced packaging technologies.
- Task 4 Programming Model report – An updated report on programmability for the architecture, including the delivery of macros, languages and compiler created.
- Task 4 Performance Models and Tools - Updated performance modeling framework, abstract layer modeling tools, and memory device modeling and benchmarking tools.

It is foreseen that analysis performed in Task 3 and Task 4 will be iterative in nature, and the performance modeling results may need to be updated.

Phase 3: Conclude

Generate final project reports summarizing the methods and technologies investigated and their impact on addressing the memory wall bottleneck while delivering energy efficiency. Reports must address all the tasks across all the of the phases of the program.

Task 5: Final Update

- Update the performance study from Phase 2, as applicable.
- Updated trade-space analysis, includes both advanced packaging and new memory technology aspects.

Task 6: Look Ahead

- Offer recommendations on promising solutions related to new memory devices and advanced packaging that could significantly enhance system performance, either for industry adoption or further research. This should include proposers plan to continue this work based on the program's results.
- Proposers' plan to create educational and trainings material to enable further research.

Deliverables:

- Final Project Report - Summarizing the methods and technologies investigated and their impact on addressing the memory wall bottleneck while delivering energy efficiency. Detailed criteria for integrating new memory and packaging technologies into existing systems, ensuring compatibility and optimal performance.
- Performance Models and Tools – Final performance modeling framework, abstract layer modeling tools, and memory device modeling and benchmarking tools.
- Project Guide - A comprehensive manual for using the new memory and packaging architectures and simulation tools, enabling researchers and developers. Guidelines for using the datasets, setup files, and simulation tools to facilitate accurate and reproducible results.
- Education Guide - Coursework and educational materials planned that demonstrate the incorporation of program learnings into academic and professional curricula.

1.5 Program Structure

The SMAP program is expected to be executed over 30 months. Due to the nature of the program, which involves multiple workloads and specialized expertise in each **Focus Area**, proposers may need to partner with other organizations towards developing a full proposal if they need help with certain **Technology Areas**. Proposers are encouraged to use the Proposers' Day to further solidify the collaborations towards building full proposal.

The Program is expected to start around December 2025. The program kickoff, interim review, final review, and monthly status meetings will provide opportunities to interact with Natcast regarding the scope of work, specifics of the technical approaches, and any technical or programmatic items of concern. In addition, one or more technical workshops open to all performers may be held during the program in which performers may provide further insights on future technical paths and challenges that must be addressed. Performer teams are encouraged to share and interact with other teams. Monthly progress teleconferences will be scheduled with the Natcast team to review technical progress and identify risks to completing the tasks outlined in the Statement of Work (SOW).

There will be several in-person reviews. Performers are expected to attend in person and should budget accordingly. The rest of the meetings will be held virtually. The first in-person review and final in-person review will be held at the performer's site. For budgeting purposes, other in-person meetings are assumed to be at the Natcast Sunnyvale, CA site. See section 1.6 for the full meeting schedule.

Table 1. In-person meeting schedule and locations

Meeting	Meeting Type	Timing	Location
1st Quarter Review	In-Person	Month 3	Performer's Site
Phase 1 Review	In-Person	Month 8	Sunnyvale, CA
Interim Review	In-Person	Month 12	Sunnyvale, CA
Interim Review	In-Person	Month 18	Sunnyvale, CA
Interim Review	In-Person	Month 24	Sunnyvale, CA
Final Project Review	In-Person	Month 30	Performer's Site

1.6 Schedule and Milestones

A SMAP program notional schedule with milestones is shown in **Figure 4**. Each proposer is expected to provide a project schedule (not exceeding 30 months) based on the scope of the proposal.

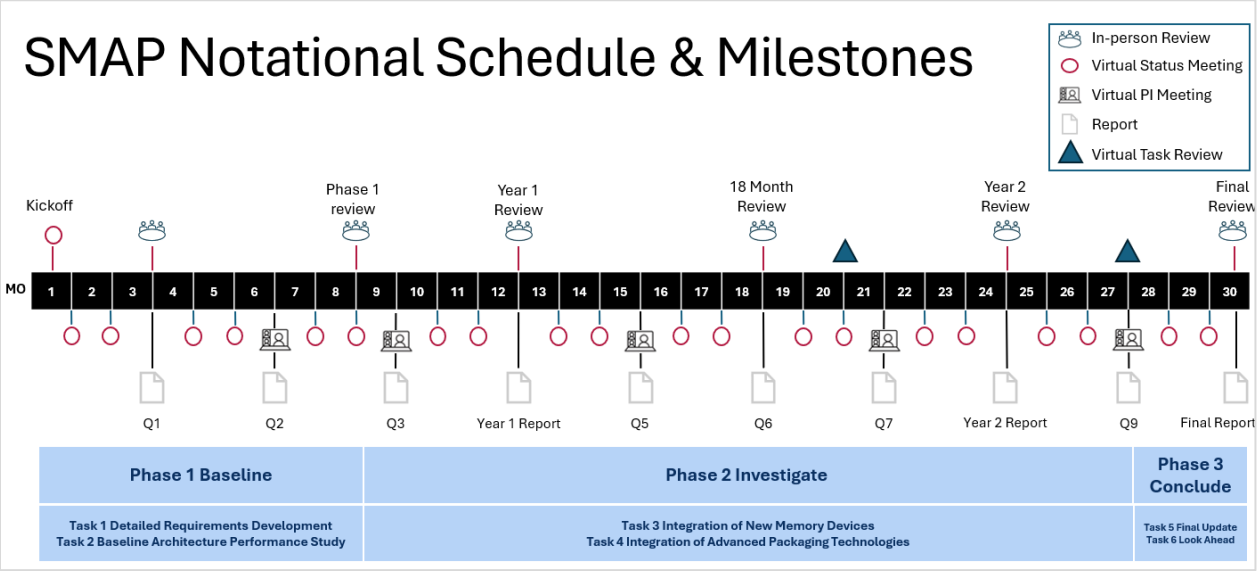

Figure 4. *SMAP Program Notional Schedule and Milestones.*

Regular meetings will be held on a monthly, quarterly, and annual basis with the performers throughout the duration of the award for the following purposes:

1. To help the performer remain current with Natcast Program Manager's (PM) insights about emerging developments in the field and other relevant developments (post-award teaming opportunities, emerging programs, etc.) related to the topic of the CFP.
2. To swiftly identify, address, and resolve any risks or challenges that could hinder a performer's ability to successfully complete the project.
3. To verify that performers are adhering to the established timelines and achieving the planned milestones; and
4. To ensure that performers are following all the necessary policies, including, as applicable, those concerning research security, intellectual property (IP) protection, and the avoidance of Foreign Entities of Concern.

Ahead of these meetings, performers are expected to submit deliverables (such as technical or programmatic status reports) to the PM to enable meaningful discussions. Furthermore, PM will facilitate group interactions among performers, either virtually or in person, to foster an appropriate exchange of knowledge among

different Projects as the phases and focus areas of the program are expected to be iterative and collaborative.

1.7 Deliverables

The list of program deliverables is shown in **Table 2**. This table includes technical and program related deliverables. These include all presentation materials from review and status meetings, including kickoff, monthly, quarterly, annual, and final written reports.

Table 2. Program Deliverables for SMAP program

Phases	Key Program Deliverables
1: Baseline	Baseline Architecture Report
	Baseline Performance Report
	Program Study Plan
	Performance Models, Tools and Data
2: Investigate	Architecture Report (Task 3 & 4)
	Performance Report (Task 3 & 4)
	Programming Model Report (Task 3 & 4)
	Performance Models, Tools, and Data (Task 3 & 4)
3: Conclude	Final Project Report
	Project Guide
	Education Plan
	Performance Model, Tools, and Data
General Program	All program related deliverables listed in Appendix D Table 10

In connection with the reporting obligations described in Section 6.3, the performer will provide to Natcast quarterly written reports that include a description of newly developed IP, including patentable inventions, data, software, and research results, as well as any applications of the developed IP.

1.8 Success Metrics

As a baseline, Natcast will use Program Management targets such as on time delivery of reports and other agreed upon deliverables, progress towards achieving milestones, and phase-specific targets to evaluate program success.

In addition to furthering progress towards the goals of the SMAP program, a successful project will demonstrate advancement by meeting or exceeding specified metrics. Success metrics for the SMAP program are divided into four key areas:

- **Technology Metrics:**
  - Identify industrially relevant metrics within the key application domain.
  - Demonstrate that the new memory architectures and simulation results meet or exceed these metrics. Demonstrate that the advanced packaging technologies and simulation results meet or exceed these metrics.
- **Data Metrics:**
  - Ensure that the data generated from architecture studies and simulations are comprehensive and well-defined.
  - Allow NSTC members to easily access and utilize structured datasets to perform accurate analyses, incorporating relevant metadata.
- **Accessibility:**
  - Demonstrate that the developed solutions, including architectures, simulation tools, and datasets, are usable across various use cases.
  - Ensure that a diverse range of stakeholders, including academia, small enterprises, and large system companies, can use these resources to advance their memory and advanced packaging related projects.
- **Documentation:**
  - Core documents should enable the use of the developed solutions post-program. These documents should include:
    - A comprehensive manual for using memory architecture and simulation tools, enabling researchers and developers.
    - Detailed criteria for integrating new memory technologies into existing systems, ensuring compatibility and optimal performance.
    - Guidelines for using the datasets and simulation tools to facilitate accurate and reproducible results.
    - Coursework and educational materials that demonstrate the incorporation of SMAP program learnings into academic and professional curricula.

More detailed target metrics are shown in the table below. For the purposes of this program, the metrics are primarily evaluated against the “threshold”, “goal,” and “stretch” targets listed below. Strong proposals should demonstrate a team’s plans and capabilities to meet or exceed the metrics stated below. Proposals may also describe additional metrics and data by which the team will demonstrate success and achievement of the goals of the SMAP program.

Table 3. Success Metrics for the SMAP Program

	Targets		
Technology Metrics	**Threshold**	**Goal**	**Stretch**
Focus Areas	At least one of the programs focus area	Address both focus areas	Extending to other industry segments
New memory device technology	Integration of at least one new memory device technology	Integration of more than one memory device technologies	Provide guidance for new memory devices research
Advanced packaging technology	Include 2D or 3D packaging option	Explore both packaging options	Provide guidance for new packaging research
Data Metrics	**Threshold**	**Goal**	**Stretch**
Performance study - Workload characteristics	FLOPS, bytes transferred from memory, operational intensity, data size	Data - locality, reuse, coherency, latency Compute - single/multi-threaded	Distributed processing, Inter-process communications
Performance study – Processing	Compute utilization, memory utilization, bandwidth, throughput, total execution time	Compute peak/sustained throughput, memory peak/sustained bandwidth, system throughput	Interprocess sustained/peak throughput, utilization
Performance study – Energy	Energy per FLOP, Energy per byte transfer, energy consumption for each module in the processing chain	Background energy, system energy	Thermal efficiency
Performance Study - Power	System peak power, processor peak power, memory peak power	Steady state compute power, steady state memory power	Leakage power, power delivery efficiency
Performance study: New memory devices	Read/write latency, energy consumption, capacity, bandwidth, utilization, density	Yield, process node, refresh power	Persistency
Performance study: Advanced packaging technologies	2D or 3D packaging types, bandwidth, latency, energy, memory capacity, area, process node	die-to-die Interconnects, routing overhead, power delivery	Thermal analysis

Trade-Space Analysis: New memory devices	Power, energy, memory capacity, memory read/write speed, bandwidth	Retention time, process node, refresh power	Fine grained sub-array, process complexity, cost
Trade-Space Analysis: Advanced packaging technologies	Power, energy, memory capacity, memory read/write speed, bandwidth, process node, area, form-factor	Fabric, die-to-die Interconnects, routing, power delivery, yield	Thermal, cost
Accessibility	**Threshold**	**Goal**	**Stretch**
Performance models and Tools	Models and tools developed adhere to industry standard practices. They should be readable, modular, maintainable and adhere to coding and framework standards	Flexible, extensible and well tested. Test results are repeatable and reproducible by 3rd party.	Comprehensive manuals and user guides
Documentation	**Threshold**	**Goal**	**Stretch**
Study reports	A comprehensive manual for using memory architecture and simulation tools, enabling researchers and developers.	Detailed criteria for integrating new memory technologies into existing systems, ensuring compatibility and optimal performance. Guidelines for using the datasets and simulation tools to facilitate accurate and reproducible results.	Coursework and educational materials demonstrate the incorporation of SMAP program learnings into academic and professional curricula.

By achieving these metrics, the SMAP Program will not only advance its stated goals but also ensure that its innovations are practical, reproducible, and accessible, thereby fostering widespread adoption and furthering progress in overcoming the memory wall challenge in the semiconductor industry.

2.0 Award Information

2.1 General Award Information

Natcast anticipates granting 8-14 awards not to exceed a total program budget for the awards of up to $33.5M. The number of awards will depend on the submissions, proposed budgets and the availability of funds. Awards will be given to proposers whose proposals best address all evaluation criteria and selection factors.

2.2 Terms and Conditions

By submitting a proposal, proposers affirm that they have read, understood, and agreed to the terms and conditions contained in the CFP.

Natcast is not obligated to make an award or award the full amount of available funds as a result of the CFP process or the receipt of proposals in response to this CFP. Natcast may remove proposers from award consideration if the parties fail to reach agreement on award terms within a reasonable time or the proposer fails to provide requested additional information in a timely manner. Funds will only be made available after entering into a binding award agreement.

As a part of the CFP process, proposals and related information submitted under the CFP may be used, extracted, copied, reproduced, and/or distributed to Natcast employees, contractors, consultants, and external reviewers, as well as the Department of Commerce or other Federal agencies and their contractors or consultants, for the purposes of conducting the competition under this CFP. Persons requiring access will be subject to appropriate non-disclosure and conflict of interest requirements.

Any parts of a proposal shared with Federal agencies may be subject to requests under the Freedom of Information Act (5 U.S.C. § 552). Proposers should designate any sections of their proposal as confidential where they contain trade secrets, privileged commercial and/or financial information.

By submitting a proposal in response to this CFP, proposers represent and warrant that they have the authority to submit a proposal and grant the rights set forth in the CFP on behalf of their organization.

2.3 Fundamental Research

Given the nature of the program, we expect a combination of both fundamental and non-fundamental research. Proposers are required to identify and provide an explanation for whether the proposed research is fundamental research or non-

fundamental research. As established by 15 C.F.R § 734.8: 'Fundamental research' means research in science, engineering, and mathematics, the results of which ordinarily are published and shared broadly within the research community, and for which the researchers have not accepted restrictions for proprietary or national security reasons.

Natcast reserves the right to make a final determination on whether the research in a specific project constitutes fundamental research and may impose additional publication or reporting terms and conditions on non-fundamental research. Proposer will be subject to pre-publication review for all publications for the duration of the program. Any publication-based non-fundamental research shall be subject to pre-publication review by NIST.

Proposers should also be aware that the content of a Research Security Plan may depend in part on whether the proposal concerns fundamental or non-fundamental research.

2.4 Research Security

2.4.1 Research Security Review and Risk Determination

Proposers are required to undergo a Research Security Review by Natcast and/or NIST in order to be considered for award. Detailed requirements are available in Appendix B and C below, which provide the information that proposers must supply for this review, including a brief summary of proposer's current capabilities related to Research Security. For initial submission, proposers must provide resumes/CVs and current and pending support forms for the Principal Investigator (PI) and Co-Principal Investigators only. Research security forms should be submitted for all other covered individuals during award negotiation after selection. A covered individual is defined as a person who contributes in a substantive, meaningful way to the scientific development or execution of a research and development project proposed.

The resulting research security risk determination may be used as a selection factor. Furthermore, Natcast may require that proposers mitigate identified risks as an aspect of award negotiation.

2.4.2 Research Security Plans

As an aspect of award negotiation, selected proposers may be asked to improve their research security practices or plans for Natcast to approve. It is essential that proposers be prepared to strengthen their research security protocols as part of the award process and/or over the course of the period of performance.

If and when selected for award negotiation, proposers must submit a detailed description of their current Research Security Plan or (if none) describe a plan to protect Natcast-funded research and associated data products. Award terms will specify that within ninety (90) days of award, proposers must show progress on implementing the Research Security Plan, and that within 180 days the research security plan must be fully implemented.

2.5 Intellectual Property and Data Rights

2.5.1 Award Agreement IP terms

The award agreement will include terms and conditions related to intellectual property and data. Certain of these terms and conditions are specifically required by Natcast's obligations to the Department of Commerce; others are intended to fulfill the NSTC mission of furthering research and engineering throughout the semiconductor ecosystem. The terms below apply only to this program; future programs may be accompanied by different terms with respect to IP.

As such, the following commitments will be required of all proposers. A performer is responsible for ensuring each member of its team and their respective affiliated organizations comply with the IP terms of the award agreement.

- **Ownership of IP:** The performer or, as applicable, the project team member responsible for development, will own all intellectual property and data developed by such performer or team member under the Project.
- **Government License:** The U.S. Government will have a nonexclusive, nontransferable, royalty-free, fully paid-up, worldwide, perpetual license to Use all deliverables, including to all inventions that are or may be patentable, developed by the performer, using government funds, during the SMAP program, for research and non-commercial purposes. The U.S. Government will not have any rights in performer's Background IP.
- **Domestic Control Restrictions:** The performer will comply with domestic control requirements adopted by Natcast pursuant to the Department of Commerce's policies under the CHIPS Act, 15 U.S.C. § 4656(g), including: (a) the owner of the inventions developed during the SMAP program that are or may be patentable under U.S. law must be a "domestic entity"—meaning, either a state, local or tribal government or a US entity with its principal place of business in the US; (b) that domestic entity—and any successor in interest—may not sell, transfer, or assign ownership of any developed inventions that are or may be patentable under U.S. law to a foreign adversary ("foreign adversary" includes any "foreign

entity of concern" and "foreign country of concern" as defined in 15 C.F.R. § 231.102, § 231.104); (c) that domestic entity may not grant a license to a foreign adversary with some limited exceptions; and (d) that domestic entity may only assign ownership of the developed inventions that are or may be patentable under U.S. law to a foreign entity (that is not a foreign adversary) after the expiration of a specified period of years; the specific period of years will be determined prior to award. While a uniform term of years, and certain disclosure requirements, will be included in all award agreements, proposers will have an opportunity to discuss the term of years prior to award.

The following IP commitments are preferred, but proposers are welcome to propose alternative terms that align with the SMAP program goals. The terms and conditions agreed upon between the selected proposers and Natcast will be included in the award agreement.

- **Rights to Use Deliverables:** The performer will grant to Natcast the rights necessary to achieve the goals of the SMAP program. The rights granted will include a non-exclusive license (with the right to sublicense to NSTC members) to use the Deliverables (as described in **Table 4**), and to practice the Related IP Rights, without the obligation to make additional payments other than the milestone payments set forth in the award agreement or as otherwise agreed to by the parties in the award agreement.
    - Natcast will consider limited exceptions to these usage rights if specifically requested in the performer's written proposal responding to this CFP.

- **Natcast Preferred IP Rights: Table 4** below includes the preferred IP rights that Natcast desires from proposers to achieve the goals of the SMAP Program. The preferred IP rights for exemplary types of Deliverables are described below:

Table 4. Program Deliverables for SMAP and preferred IP rights.

Phases	Key Program Deliverables	Preferred IP Terms
1: Baseline	Baseline Architecture Report	1
	Baseline Performance Report	1
	Program Study Plan	1
	Performance Models, Tools and Data	2
2: Investigate	Architecture Report	1
	Performance Report	1
	Programming Model Report	1

	Performance Models, Tools and Data	2
3: Conclude	Final Project Report	1
	Project Guide	1
	Education Plan	1
	Performance Models, Tools and Data	2
General Program	Reports, Presentation Material, Documentation, Developed Curriculum	1

1. The datasets, test results, reports, presentation materials, guidance and recommendations, developed curriculum, and other related content or documentation developed during the SMAP program may be included in a Natcast controlled repository and made available to current and future NSTC members for R&D and non-R&D purposes. The performer is required to provide useful deliverables to Natcast, but may, with Natcast's approval, remove specific data or information that would reveal sensitive, proprietary information.
2. Any software and models developed should be made available for Natcast future research programs and sub-licensable by Natcast to current and future NSTC members for R&D purposes. The performer may propose commercial terms for licensing fees that Natcast or NSTC members would need to pay to use the software for commercial purposes. The reasonableness of these commercial terms will be a criterion in evaluating the proposal.

2.5.2 Definitions for IP and Data Rights Terms

For purposes of this Section 2.5, the following terms (whether capitalized) have the following respective meanings:

"Background IP" means any pre-existing IP or IP developed independently of the SMAP program.

"Deliverables" means materials and information provided, or required under the award agreement to be provided, to Natcast or NSTC members in connection with the SMAP program.

"IP" and "intellectual property" means all intellectual property, intellectual property rights and other proprietary rights, including copyrights; software, written materials and other works of authorship; other rights in software; data, databases and rights in data and databases; reports, curriculum, or white papers; patents, patent applications and rights with respect to inventions; trade secrets and other information and ideas not generally known to the public; and methods, processes, algorithms and other subject

matter of intellectual property or other proprietary rights. "IP" and "intellectual property" do not include trademarks and related rights unless otherwise specified. This definition does not apply to references to IP or Intellectual Property under 15 U.S.C. § 4656(g).

"Related IP Rights," in reference to Deliverables, means IP embodied in or necessary for use of the Deliverables.

"Use," with respect to Deliverables or IP, means to utilize, reproduce, distribute, disclose, modify, and make and supply products or services using, such Deliverables or IP, and otherwise use such Deliverables and IP. This definition does not apply to references to use by the U.S. Government.

2.6 Domestic Production

To promote a robust, sustainable domestic capacity for semiconductor R&D, prototyping, and production, and pursuant to the CHIPS Act domestic production requirements (15 U.S.C. §4656(g)), CHIPS R&D requires proposers to develop plans to domestically produce, to the extent possible, any intellectual property resulting from CHIPS-funded microelectronics research and development.

For the purposes of 15 U.S.C. § 4656(g):

- "Intellectual property" means any invention that is or may be patentable under U.S. law.
- "Production" includes the manufacture, integration, assembly, testing, and packaging of semiconductors, materials used to manufacture semiconductors, or semiconductor manufacturing equipment (e.g. memory cells, memory devices, packaging developed or improved as a result of CHIPS-funded intellectual property.

The domestic production provisions are central to the CHIPS Act's mission of strengthening America's semiconductor ecosystem and reducing reliance on foreign manufacturing capabilities. By ensuring that innovations developed through NSTC funding are manufactured domestically when feasible, the program aims to create a complete innovation-to-production pipeline within the United States. NSTC recognizes that certain production activities may face challenges in domestic implementation due to various factors including specialized manufacturing capabilities, cost considerations, or market dynamics. The evaluation process will consider the reasonableness and thoroughness of domestic production plans within the context of each proposal's specific technologies and commercial applications.

Natcast does not anticipate that the Domestic Production requirement will be applicable to this program, given the nature of the research. Since the intellectual property resulting from this funding opportunity is expected to be used primarily for the creation of software, the definition of "production" is not relevant to the proposed activities. Therefore, a Commercial Viability and Domestic Production (CVDP) plan is not required for the submission of proposals.

3.0 Eligibility Information

The recipient of an award must be a core, rather than an affiliate, member and all subawardees must also be core NSTC members at the time of award.

NSTC Members may not be foreign entities of concern or foreign countries of concern, as those terms are defined in 15 C.F.R. 231.104 and 231.102, respectively.

Individuals and unincorporated sole proprietors are not eligible to receive funding or for NSTC membership. Moreover, as also required by this CFP, recipients must undergo a Research Security Review (see 2.4.1) and be prepared to implement a Research Security Plan (see 2.4.2).

All awardees and subawardees must be a domestic entity to be eligible for an award. A domestic entity is one that is incorporated within the United States (including U.S. territories) and with its principal place of business in the United States (including U.S. territories). Additional information on participation by foreign entities can be found in Section 3.5 "Foreign Collaboration and Overseas Activities. Additional information about NSTC Membership and the process for becoming a member is available at https://natcast.org/nstcmembership.

3.1 Federal Entities

Federal Entities (*e.g.*, Federal departments and agencies, military services educational institutions, etc.) are eligible to participate in funding opportunities as team members or contractors, to the extent allowed by law and subject to applicable direct competition limitations. Federal Entities must clearly demonstrate that the work is not otherwise available from the private sector and provide written documentation citing the specific statutory authority and contractual authority, if relevant, establishing their ability to receive Federal award funds and compete with industry. Proposers must identify the Federal entity in the Project Plan and provide documentation attached to the required letter of commitment establishing that the Federal entity is able to participate in the proposed work.

Federally Funded Research and Development Centers (FFRDCs) may participate in awards as subawardees or contractors, to the extent allowed by law, based on the unique and specific needs of the project. Proposers must identify the FFRDC(s) in the Project Plan and provide documentation attached to the required letter of commitment establishing that FFRDC subawardees and contractors are able to participate in the proposed work, including:

- Documentation demonstrating that the proposed work does not compete with the private sector; and
- Documentation from the FFRDC's sponsoring institution citing the FFRDC's eligibility to participate in competitive government funding opportunities; the FFRDC's compliance with the sponsor agreement; and confirmation from the sponsoring agency that they can receive Federal funds from Natcast.

3.2 Eligible Use of Funds

Eligible uses may include, but not be limited to, basic and applied research, demonstration, prototyping, preparation of commercial viability and domestic production information, industry stakeholder engagement, design work, information collection, acquisition of software or hardware, manufacturing costs, associated program travel, data analysis, audit costs, and contracted work.

Use of funds for travel costs must be consistent with the following guidelines. Permissible Costs include necessary and reasonable costs for travel to perform the scope outlined in the projects. For common carrier transportation costs, performer shall agree that it will travel by a direct route or on an uninterrupted basis (*i.e.*, travel will not be interrupted for personal convenience). In addition, travel will be by coach class, except for instances in which Natcast has provided written approval. Non-coach class travel is expected to be rare, and Natcast may utilize the standards in 41 C.F.R. § 301-10.103 to determine whether, in their discretion, to approve other than coach class transportation. For meals and incidental expenses, the per diem rates established by the Federal Travel Regulation are to be utilized. For lodging, proposers should plan to book reasonable but not extravagant lodging accommodations for employees in travel status. Proposers should make use of government rates whenever possible; otherwise, corporate rates or other discounts should be obtained whenever possible. For air travel, performer shall use U.S.-flag air carriers to the extent the carriers provide those services, consistent with the Fly America Act at 49 U.S.C. § 40118.

Proposers may also propose to expend limited funds to protect innovations or content developed under the funding opportunity, such as fees for patent or copyright protection or to enhance research security.

3.3 Organizational Conflict of Interest

Proposers are asked to identify any potential organizational conflicts of interest that may arise in the context of this CFP, and (if applicable) potential strategies that it proposes to mitigate those conflicts.

3.4 Cost Sharing

Cost sharing is encouraged but not required for this effort. It is neither an evaluation nor selection criterion.

3.5 Foreign Collaboration and Overseas Activities

Foreign entities (*i.e.* for-profit companies, educational institutions, and other non-profits) and foreign individuals (*i.e.* persons participating from a foreign location) can participate in the SMAP Program on an unfunded basis, subject to certain limitations such as a research security review, to ensure the protection of CHIPS R&D-funded intellectual property from foreign adversaries. Non-U.S. citizens whose work will occur in the U.S., and who are lawfully present and authorized to work in the U.S., are eligible to participate on a funded basis, subject to any export control laws and regulation.

To protect national security and the resiliency of supply chains, however, foreign entities of concern may not receive CHIPS R&D funds or participate in NSTC R&D programs. Foreign entities of concern ("FEOCs") include entities owned by, controlled by, or subject to the jurisdiction or direction of the governments of China, Russia, North Korea, or Iran. Complete definitions of foreign entity of concern and foreign country of concern are found at 15 CFR part 231.

Foreign entities that are not FEOCs may participate, on a funded basis, as members of a project team, as subawardees or contractors, subject to Natcast approval. The proposer must provide Natcast with a written justification demonstrating that the foreign entity's involvement is essential to advancing project objectives, such as by offering access to unique facilities, IP, or expertise that is otherwise not readily available in the United States. Natcast will only approve work outside of the United States if Natcast determines it is in the best interest of CHIPS R&D and the United States, including the domestic economy generally, U.S. national security, U.S. industry, or U.S. manufacturing competitiveness. Natcast's determination regarding the performance of

project tasks outside the United States may be based on information provided by the proposer and by other Federal agencies.

A foreign entity is any entity that is not a domestic entity. A domestic entity is one that is incorporated within the United States (including U.S. territories) and with its principal place of business in the United States (including U.S. territories).

4.0 Proposal and Submission Information

4.1 General Information

The SMAP proposal and award is comprised of five stages:

Step 1: Concept paper submission is required.

Natcast will respond to proposers encouraging or discouraging the submission of a full proposal.

Step 2: Full proposal submission

Step 3: Full proposal selection by Natcast

Step 4: Award agreement negotiation between Natcast and selected proposers

Step 5: Award and Program Kick-Off

Submission of a concept paper is required for submission of a full proposal. Concept papers may be up to 3 pages long for each **Focus Area** proposed. If applying for multiple **Focus Areas**, a separate concept paper must be submitted for each **Focus Area**. Recipients will receive feedback encouraging or discouraging a full proposal within 14 days of concept paper submission. No down-selection will occur. All proposers who submitted a concept paper will be able to advance to full proposal if they choose. A concept paper template is provided separately, at https://natcast.org/research-and-development/smap while submission guidelines and requirements are presented in Appendix B.

Proposing teams should include members capable of successfully completing the program as defined and subsequently transitioning the deliverables for the benefit of the NSTC members. Teams should possess:

- In-depth knowledge and experience with new memory devices and their integration.
- Proven experience in modeling and implementing 2.5D and 3D packaging solutions.

- Ability to profile and optimize architectures for industry-relevant workloads.
- Ability to understand and devise solutions to address programmability challenges.
- Capability to collaborate effectively with other teams, share knowledge, and contribute to a collective goal.

The composition of the team can change between concept paper submission and proposal submission. Concept paper submissions will be evaluated against the first two criteria laid out in Section 5.1: Evaluation Criteria. Concept papers may be submitted directly by any individual who is authorized to agree to the submission terms and conditions on behalf of the organization submitting a proposal.

Natcast will only encourage full proposals for technologies that have been proven at a TRL of 3 or higher (**Figure 5**). This means that all research proposed should already have had basic concepts and principles observed and reported, the technology concept and application has been formulated, and analytical and experimental critical function and/or characteristic proof of concept has been demonstrated and validated. We do not recommend submitting any proposals with new memory and advanced packaging technologies at TRL levels 1-3.

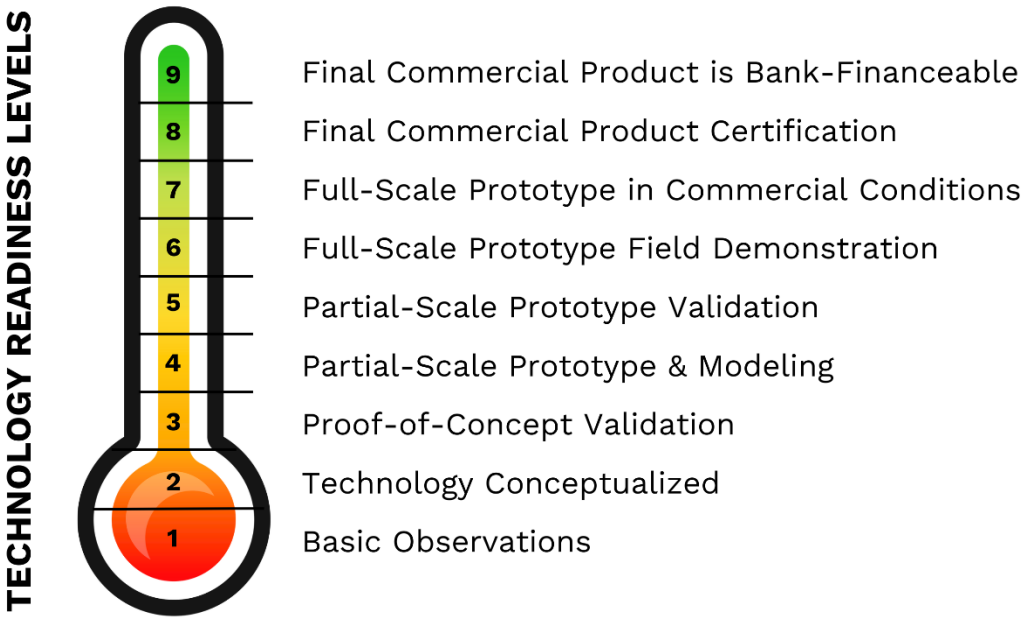

Figure 5. *Technology Readiness Levels (TRL) explained.*

The concept paper and the full proposal must be uploaded to a secure web site: https://natcast.secure-platform.com/rnd. It is also possible to navigate to this site from the SMAP home page: https://natcast.org/research-and-development/smap.

4.2 Proposal Form and Content

Full proposals are required to adhere to the Project Narrative template, see separate attachment on the SMAP home page at https://natcast.org/research-and-development/smap, and include a Budget Workbook and Quad Chart Summary. Page limitations and proposal submission requirements are explained in Appendix B and C below.

Full proposals must contain the following:

1. **Project Narrative**

See Appendix B and C below for more detailed requirements and suggestions.

- Cover Page
- Executive Summary
- Goals and Impact
- Management Plan
- Technical Plan
- Intellectual Property Rights Management Plan
- Appendices
  - Table of Abbreviations and Acronyms
  - Bibliographic List of References
  - Table of Funded Participants and Unfunded Collaborators
  - Statement of Work (SOW)
  - Domestic Production Plan
  - Letters of Commitment
  - Research Security Capabilities
  - Resumes/CVs [Only for PI and Co-PI(s) during proposal]
  - Current and Pending Support Forms [Only for PI and Co-PI(s) during proposal]

2. **Budget Workbook**

The budget workbook is an Excel-format document, uploaded separately from the Project Narrative. Budget template will be made available for the convenience of proposers at the SMAP home page: https://natcast.org/research-and-development/smap

3. **Quad Chart Summary**

As part of the proposal submission process, applicants are required to include a Quad Summary page that provides a comprehensive yet concise visual overview of the project. This single-page document in landscape orientation serves as an executive summary, highlighting the program overview, key visual representations, budget information, and essential team details. Please follow the template, available at the SMAP home page, and formatting requirements to ensure the submission meets all guidelines.

4.3 Teaming

It is anticipated that this effort will be led by teams including partnerships between combinations of university proposers, start-ups, commercial laboratories, facilities, and companies. Teams may include unfunded collaborators. This program anticipates funding multiple collaborative teams of various sizes with varying scopes (*i.e.*, addressing either one or both **Focus Areas**), start-ups, commercial laboratories, facilities, and companies.

Teams should be comprised of one lead proposer (the "performer") with funded team members from entities different than the performer who may be considered subawardees and/or unfunded collaborators. Subawardees and collaborators must meet eligibility requirements and should submit a teaming letter with the project proposal or white paper, as applicable. Full proposals should include a subawardee budget in addition to letters of commitment. A single entity may only submit a maximum of two (2) proposals (one to each **Focus Area)** as the lead proposer but may participate on more than two teams as subawardees or unfunded collaborators.

4.4 Frequently Asked Questions

Proposers can submit questions by May 13, 2025, to smap@natcast.org. Abstracted answers will be shared publicly via FAQ posted at https://natcast.org/research-and-development/smap.

5.0 Proposal Review Information

5.1 Evaluation Criteria

Proposals will be evaluated according to the following criteria, listed in order of priority:

- **Overall Scientific and Technical Merit** - This criterion addresses the quality, innovativeness, and feasibility of the project proposal and the potential for meeting

the objectives of the funding opportunity. Reviewers will consider the extent to which:

- The proposed activities are innovative, original, or potentially transformative;
- The proposal demonstrates knowledge of the current state of the art in relevant fields and the feasibility of the proposed technologies to be advanced, including gaps, constraints, and significant challenges that must be addressed;
- The plans for achievements, outcomes, or goals represent a significant advance relative to the state of the art globally in the field of technology development, exploration, and transfer;
- The proposed plans rely on the use of proven and reliable methods or processes which have been shown to work in the past but had not otherwise been generally applied in industry-relevant conditions or environments; and
- The extent to which the proposed methodology and technology could lead to a fundamental advancement in science, knowledge, and understanding which would otherwise not occur.

- **Utility and Benefit to NSTC Membership** - This criterion addresses the potential utility and benefits of the proposed projects to Natcast and the NSTC membership or plans for making the NSTC membership aware of the emerging knowledge and enabling its use. Reviewers will consider the extent to which:
  - The overall accessibility of the methodology or technology to potential interested users;
  - The extent to which the proposed IP terms will make rights in data, inventions, and copyrightable material available to the NSTC membership;
  - The extent to which any proposed additional IP benefits are commensurate with the benefit of Natcast funding and the availability of NSTC infrastructure and support.
  - The strength of the commercialization plan for Natcast-funded inventions, datasets, and copyrightable materials; and
  - The reasonableness of the IP terms to enable Natcast and NSTC members to gain access to the deliverables generated in connection with the SMAP program.

- **Transition and Impact Strategy** - This criterion addresses the project's potential for supporting the commercialization and domestic production of funded semiconductor innovations, as well as beneficial impacts to workforce development and the broader domestic research, development, and innovation ecosystem. Reviewers will consider the extent to which the proposal provides:

- A methodology or technology capability which impacts an important area of fundamental sustainability research for the semiconductor industry
- A reasonable approach for transitioning the proposed technology to commercial deployment, including specific milestones and timelines
- The potential for which the proposed methodology and technology can be utilized by a broad user base, supported by concrete user engagement strategies
- Documentation of how technical integrations will be achieved and maintained throughout the project lifecycle

If proposers include developing training materials or curriculum (e.g., 2-hour virtual training module related to the technical area of the proposal) in their proposal, the intent is that these materials can be delivered to NSTC Workforce Center of Excellence for broader distribution. Success metrics must include both quantitative and qualitative measurements.

All training material and curriculum created under the SMAP program should be made available under a Creative Commons Attribution (CC BY 4.0) license (https://creativecommons.org/licenses/by/4.0/). The content will be uploaded to NSTC's workforce repository to support workforce development and other training and educational efforts.

If curriculum development or training is included, proposers must complete the curriculum mapping table provided:

Table 5: Curriculum or Training Components for SMAP

Curriculum Component	Core Skills Addressed	Key Competencies
[Component Name]	[Skills]	[Competencies]

Proposers shall include workforce development updates as a standing agenda item in their regular quarterly program review meetings.

- **Project Management** - This criterion addresses the degree to which proposers demonstrate that they have the appropriate personnel, experience, and access to required equipment and facilities. Reviewers will consider the extent to which:
  - The proposal identifies key staff, leadership, and technical experts with qualifications and experience appropriate to the proposed work, including prior experience and results in efforts similar in nature, purpose, or scope of proposed activities; and

- The proposed activities are feasible, well organized, and conceived clearly and realistically.

5.2 Selection Criteria

Natcast will select a portfolio of proposals based on a broad range of criteria including:

- **Merit Review** - Results of the merit reviewers' evaluations, including narrative evaluations (if applicable), and the reviewers' adjectival ratings (if applicable).
- **Relevance to Program and Mission** - Alignment with the objectives and priorities of NSTC and the mission, goals, and priorities of the NSTC R&D program. This may include considerations related to research security, domestic production, and domestic control of intellectual property.
- **Funding** - The availability of funding.
- **Variation among Projects and Participants -** The degree to which the selected portfolio of proposed teams and project provides for a variety of proposed project topics or approaches, geographical variation among participants, and institutional variation (including small and medium enterprises, universities, nonprofit research organizations, etc.) in the overall NSTC projects portfolio.
- **Funding Duplication**. Selection will strive to avoid funding duplicative projects.
- **Benefit to NSTC Membership**. The extent to which IP plans and other factors benefit the NSTC membership, as described in Section 5.1.
- **Research Security Risk**. Natcast may consider the results of the Research Security Review in its selection.

5.3 Review of Proposals

The review process involves evaluation of each conforming and eligible proposal based on its individual merits, followed by a selection process that considers a range of broader criteria that are comparative and/or additive of the merit evaluation as Natcast determines which set of proposals best meets the program objectives.

Natcast may, at its discretion, review a partially complete proposal if any gaps in information can be rectified easily during the review or award process for completion of the proposal.

6.0 Award Administration Information

6.1 Notification of Submission Status

Natcast intends to publicly announce awards no later than thirty (30) days after all awards under this CFP are executed. Announcements may occur earlier once both parties give consent to announce the award. Any early announcements must reflect that a final, binding award has not yet been made.

Selected proposers will be notified by email when a determination has been made, and they will advance to the next phase: award negotiations.

Proposers who have not been selected will also be notified by email and may be offered the opportunity to receive a debriefing after the funding opportunity is officially closed, as determined by Natcast. Proposers must request for a debrief from Natcast within 14 business days of the email notification. Natcast will then work with such proposers to schedule a date and time for the debrief.

6.2 Policy Requirements

6.2.1 Documentation Retention

Proposers must keep and retain records of all data generated through funded research which includes but is not limited to technical data, specifications, software, and pilot designs. In addition, proposers must keep and retain all financial records, supporting documents, statistical records, and other materials related to the award.

These requirements apply for three (3) years following Natcast's final payment.

6.2.2 Tangible Property

The acquisition of certain tangible personal property, including equipment and supplies, must comply with the requirements of 2 C.F.R. § 200.313 and 314. Proposers will also be required to record appropriate notices of record to indicate that personal property has been acquired or improved with federal funds and that use and disposition conditions apply to the property, in accordance with 2 C.F.R. § 200.316. For purposes of this CFP, these requirements apply to tangible personal property (including information technology systems), including equipment and supplies, having a useful life of more than one year and a per-unit acquisition cost which equals or exceeds the lesser of the capitalization level established by the acquiring entity for financial statement purposes, or $10,000. Equipment installation and any associated construction costs may be allowable, contingent on Natcast prior approval. Permissible equipment installation and

associated construction costs are expected to be minimal (*e.g.* likely below $100,000.00). If approved, such costs may require compliance with laws and regulations relating to federally funded construction projects and environmental requirements.

Certain tangible assets, specifically any property which may be generally considered "customer owned tooling" which are wholly or partially acquired through the use of program funds may, in some cases, be expected to be transferred to Natcast at the end of the program to be managed for the benefit of NSTC members.

Proposers may not use award funds to acquire real property or to engage in construction and not expect to be in the scope of SMAP.

6.2.3 Accounting Standards

Award agreements will require that Proposers maintain proper GAAP accounting of all federal funds provided under the award, including the use of funds for approved research and development purposes as well as maintain its commitment to any cost-sharing, if applicable.

6.3 Reporting

The number and types of reports will be specified in the award agreement but will include at a minimum quarterly technical and financial status reports, a final project report and post project reports.

- **Technical Reports -** These reports should provide Natcast Program Managers with information on the progress of supported projects and the way funds are being used. Technical reports may request the types of information described in the illustrative Technical Report Template found in *Appendix C*.
- **Final Project Report -** This last report of the project should be written specifically for the most recently completed budget period. It should address progress in all activities of the project in its final year, including any activities intended to address the Broader Impacts criterion that are not intrinsic to the research. Illustrative contents of this report are outlined in *Appendix D*.
- **Post Project Reports -** Once the project is completed, proposers must comply with recordkeeping and reporting obligations required by Natcast for compliance with 4656(g) and tracking IP.

6.3.1 Meeting and Travel Requirements

Please refer to Section 1.6 for travel expectations. Proposers should anticipate travel costs accordingly.

6.4 Federal Requirements

Awards made under this CFP are made from federal funds that Natcast receives under an "other transaction agreement" (OTA) with the Department of Commerce. These funds are generally not subject to the Uniform Administrative Requirements, Cost Principles, and Audit Requirements for Federal Awards, 2 C.F.R. Part 200, or the Federal Acquisition Regulation. They are subject to requirements imposed via the OTA. The OTA requires that awards under this CFP include terms addressing the following:

- A prohibition on federal funds going to any foreign entities of concern or foreign countries of concern, as those terms are defined in 15 C.F.R. 231.104 and 231.102, respectively, or to any other entity debarred, suspended or otherwise prohibited from receiving federal funds;
- Compliance with export control laws; including providing to Natcast, a Technology Control Plan (TCP) when during the program, proposer produces or accesses technology and technical data controlled under United States Export Control Laws and Regulations;
- Compliance with security and privacy controls; including reporting to Natcast suspected or actual cyber incidents and Natcast confidential information related to the program;
- A prohibition on federal funds going to the purchase of real property;
- U.S. government rights in the project deliverables;
- NIST prepublication review of non-fundamental research topics;
- Research security;
- Domestic production and control;
- Compliance with Title VI of the Civil Rights Act, Title IX of the Education Amendments, and other non-discrimination laws that prohibit discrimination on the basis race, color, national origin, handicap, age, religion, veteran status, or sex;
- Maintaining effective internal controls;
- Providing access to records for examination, audit, investigation, or inspection by Natcast, the Department of Commerce, a third party retained by the Department of Commerce, the Department of Commerce Office of Inspector General, or the Comptroller General. This requirement continues to apply for three (3) years after the final award payment, unless otherwise required by law;
- A certification to the best of its knowledge and belief that no Federal appropriated funds have been paid or will be paid to any person for influencing or attempting to influence an officer or employee of any agency, a Member of Congress, an officer or

employee of Congress, or an employee of a Member of Congress on its behalf in connection with the making of an award under this CFP.

- For award funded travel, adherence to the Fly America Act at 49 U.S.C. § 40118, economy class travel 41 C.F.R. § 301-10.103, and GSA per diem and hotel rates (https://www.gsa.gov/travel/plan-book/per-diem-rates) as otherwise provided by Natcast.

These requirements and others will be specified in award terms. Proposers will be subject to sub-recipient monitoring throughout the life of the award, which will include steps to ensure that proposers comply with applicable requirements.

6.5 Payment Terms

The SMAP program plans to implement the following payment structure:

Initial Payment - Upon signing the award agreement, an initial payment of 15% of the total award value will be made to the awardee.

Milestone Payments - Payments will be made upon the completion of predefined milestones. These milestones and their associated payments will be clearly defined in the contract or agreement.

Final Payment - A final payment constituting no less than 15% of the total contract value will be made upon the acceptance of the final report by Natcast.

All payments, including milestone and final payments, will be subject to the approval of the designated Program Manager (PM) following Natcast's approval process flows and will be paid within 45 days of approval of the milestone.

7.0 Appendices

7.1 Appendix A: Acronyms, Definitions and Citations

7.1.1 Acronyms

- **ADK** – Assembly Design Kit
- **AI/ML** – Artificial Intelligence/Machine Learning
- **BW** – Budget Workbook
- **CFP** – Call for Proposal
- **CHIPS** – Creating Helpful Incentives to Produce Semiconductors
- **CoC** – Chip-on-Chip
- **CoW** – Chip-on-Wafer

- **CPU** – Central Processing Unit
- **CPSF** – Current and Pending Support Forms
- **DRAM** – Dynamic Random Access Memory
- **DTCO** – Design-Technology Co-Optimization
- **EDA** – Electronics Design Automation
- **FeFET** – Ferroelectric Field Effect Transistor
- **FeRAM** – Ferroelectric Randon Access Memory
- **FLOPS** – Floating Point Operations per Second
- **FPGA** – Field Programmable Gate Array
- **GPU** – Graphics Processing Unit
- **HDI** – High-Density Interconnects
- **IP** – Intellectual Property
- **MRAM** – Magnetic Random Access Memory
- **NPU** – Network Processing Unit
- **NSTC** – National Science and Technology Council
- **PCM** – Phase-Change Memory
- **PI** – Principal Investigator
- **PM** – Program Manager
- **PoP** – Package-on-Package
- **RRAM** – Resistive Randon Access Memory
- **SMAP** – Scalable Memory Architecture Program
- **SOW** – Statement of Work
- **SRAM** – Static Random Access Memory
- **STCO** – System-Technology Co-Optimization
- **STT-MRAM** – Spin Transfer Torque Magnetic Random Access Memory
- **TCB** – Thermal Compression Bonding
- **TSV** – Through-Silicon Vias
- **TRL** – Technology Readiness Level

7.1.2 Definitions

- **Collaborator –** An unfunded entity, or individual, that provides property, equipment, subject matter expertise, or other assistance in connection with the SMAP program.
- **Contractor –** An entity, who is not a subawardee, from whom the Awardee purchases property, equipment, or who provides to Awardee subject matter expertise or consultative services needed to carry out an Awardee program but has limited programmatic involvement in the Award program.

- **Covered Individual –** The CHIPS and Science Act defines a "covered individual" as an individual who (A) contributes in a substantive, meaningful way to the scientific development or execution of a research and development project proposed to be carried out with a research and development award from a Federal research agency; and (B) is designated as a covered individual by the Federal research agency concerned. *(Refer to CHIPS for America FAQs.)*
- **Fundamental Research -** basic and applied research in science and engineering, the results of which ordinarily are published and shared broadly within the scientific community, as distinguished from proprietary research and from industrial development, design, production, and product utilization, the results of which ordinarily are restricted for proprietary or national security reasons, according to NSDD 189.
- **Subawardee** - An entity that is not the prime awardee that carries out a defined portion of a program's scope of work. Performs a substantive portion of the programmatic work and is directly engaged in carrying out specific objectives of the program award as detailed in the statement of work (SOW) and budget. Subawardee personnel may be included as Co-PIs and/or Key Personnel in the Award program
- **New Memory Devices:** Memory devices that utilize new bit-cell technology other than those used in SRAM, DRAM and Flash memory demonstrated to be TRL>3 phase
- **Operational Intensity**: FLOPS/Bytes – floating point operations executed for bytes transferred from main memory

7.1.3 Citations

[1] "A Vision and Strategy for the NSTC." Accessed: Jan. 30, 2025. [Online]. Available: https://www.nist.gov/system/files/documents/2023/04/27/A%20Vision%20and%20Strategy%20for%20the%20NSTC.pdf

[2] O. Mutlu, S. Ghose, J. Gómez-Luna, R. Ausavarungnirun, M. Sadrosadati, and G. F. Oliveira, "A Modern Primer on Processing in Memory," Feb. 06, 2025, *arXiv*: arXiv:2012.03112. doi: 10.48550/arXiv.2012.03112.

[3] "Decadal Plan for Semiconductors - SRC." Accessed: Feb. 06, 2025. [Online]. Available: https://www.src.org/about/decadal-plan/

[4] Shuhan Liu *et al.*, "Future of Memory: Massive, Diverse, Tightly Integrated with Compute – from Device to Software", [Online]. Available: https://tinyos.stanford.edu/papers/liu24iedm.pdf

[5] A. Boroumand *et al.*, "Google Neural Network Models for Edge Devices: Analyzing and Mitigating Machine Learning Inference Bottlenecks," Accessed: Jan. 28, 2025. [Online]. Available: https://www.computer.org/csdl/proceedings-article/pact/2021/427800a159/1xNNsPp0Dny

[6] A. Gholami, Z. Yao, S. Kim, C. Hooper, M. W. Mahoney, and K. Keutzer, "AI and Memory Wall," *IEEE Micro*, vol. 44, no. 3, pp. 33–39, May 2024, doi: 10.1109/MM.2024.3373763.
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[8] "Benchmark Work | Benchmarks MLCommons," MLCommons. Accessed: Apr. 01, 2025. [Online]. Available: https://mlcommons.org/benchmarks/
[9] *KULeuven-MICAS/zigzag*. (Mar. 29, 2025). C++. MICAS (KU Leuven). Accessed: Apr. 03, 2025. [Online]. Available: https://github.com/KULeuven-MICAS/zigzag
[10] *NVlabs/timeloop*. (Apr. 01, 2025). C++. NVIDIA Research Projects. Accessed: Apr. 03, 2025. [Online]. Available: https://github.com/NVlabs/timeloop
[11] *maestro-project/maestro*. (Mar. 31, 2025). MATLAB. MAESTRO Project. Accessed: Apr. 03, 2025. [Online]. Available: https://github.com/maestro-project/maestro

7.2 Appendix B: List of Submission Documents

7.2.1 Proposal Formatting Requirements

- Naming convention requirement:
  - Please include [OpenWater Application #] in the title of the Proposal submission document(s).
- Font:
  - Use one of the following fonts:
    - Arial (not Arial Narrow), Times New Roman, or Calibri at a font size of 12 points or larger; or
    - Aptos or Computer Modern family of fonts at a font size of 11 points or larger.
    - Font size 10 pt should be used for tables and figures.
- Line spacing: Single
- Margins: One (1) inch top, bottom, left, and right
- Page layout: Portrait orientation
- Paper size: 8.5" by 11"
- Application language: English
- File format: All applications must be typed, in English, in a .docx or .pdf format.
- Page Limit: see Table 6 and Table 7 below

Table 6. Concept Paper Page Limit

Section	Page Limit	Additional Details
Concept Paper	3 pages	Submit separate concept papers for each **Focus Area**

Table 7. Proposal Submission Page Limit Requirements

Section	Page Limit	Additional Details
Base Proposal	20 pages	Includes: executive summary, goals and impact, management plan, technical plan, fundamental research declaration, proposed international collaborations, and IPMP sections
Appendices (Refer to Section 7.3.2)	Not counted	Excluded from page limit
Multiple Focus Areas	Separate concept paper and Proposal required	Separate concept paper and proposal must be submitted for each **Focus Area** (e.g., Data Center and Edge)
Multiple Solutions per *Task Area*	No additional pages allowed	Clearly delineate each subtask within the proposal

B.1 Concept Paper

This section is designed to help proposers prepare their concept papers for submission. Concept papers are limited to 3 pages or less with separate submissions required for each **Focus Area**.

Table 8. Concept Paper Document Requirements

Proposal Submission Component	Page Limit	Format Requirements
Cover page	Not included in page count	Refer to Concept Paper Template for Cover Page at https://natcast.org/research-and-development/smap
Executive Summary	Included in page count	Concise overview of technical approach highlighting innovative aspects related to the Focus Area.
Overall Scientific and Technical Merit	Included in page count	Description of proposed advances relative to state of the art with measurable goals and scientific impact.
Utility and Benefit to NSTC Membership	Included in page count	Summary of benefits, accessibility strategy, and IP approach to maximize commercialization potential.
Estimated Budget	Included in page count	Provide a high-level estimated budget breakdown per phase.
Glossary / References	Not included in page count. References are limited to 1 page max.	Include glossary of terms and references of key publications, white papers, and/or technical documents from the team that demonstrate expertise in the relevant area.

B.2 Project Narrative

This section establishes the framework for proposers to present their technical approach, project management strategy, and expected outcomes in response to this solicitation. Each proposal must thoroughly address all components outlined below, demonstrating a clear understanding of the technical challenges and a well-defined pathway to achieving the stated objectives. **Table 9** below provides high-level requirements for each submission component; however, proposers should refer to Section 7.3.1 and 7.3.2 for detailed information on content expectations. Proposers should designate any sections of their proposal as confidential where they contain trade secrets, privileged commercial and/or financial information.

Table 9 – Project Narrative Document Requirements and Page Limits

Proposal Submission Component	Page Limit	High Level Format Requirements
Cover Page	Not included in page count	• Refer to Project Narrative Template for Cover Page at https://natcast.org/research-and-development/smap
Executive Summary	Included in page count	• Concise overview of project objectives, methods, and potential impact.
Goals and Impact	Included in page count	• Description of project outcomes, benefits to NSTC membership, and IP commercialization strategy.
Management Plan	Included in page count	• Overview of team structure, coordination approach, and risk management strategies.
Technical Plan	Included in page count	• Detailed approach to technical challenges with measurable milestones and risk mitigation.
Fundamental Research Declaration	Included in page count	• Identification of fundamental research activities with supporting rationale.
Proposed International Collaborations	Included in page count	• Justification and compliance information for any foreign partnerships.
Intellectual Property and Rights Management Plan	Included in page count	• Refer to Project Narrative Template for the IPMP Plan at https://natcast.org/research-and-development/smap.
Table of Abbreviations and Acronyms	Not included in page count	• Alphabetical list of all abbreviations, acronyms, and their meanings.
Bibliographic List of References	Not included in page count	• Limit to 1 page.

Table of Subawardees and Unfunded Collaborators	Not included in page count	• Alphabetically ordered list of all team members, funded and unfunded, including known contractors.
Statement of Work (SOW)	Not included in page count	• Structured breakdown of tasks, methods, and deliverables aligned with budget items. Numbering must correspond directly to budget line items.
Budget Workbook	Not included in page count	• Separate document aligned with SOW. To be uploaded separately as an excel spreadsheet, using the Natcast approved Budget Workbook (BW) available at https://natcast.org/research-and-development/smap • Alteration of the rows / columns in Budget Workbook template is prohibited except for the Milestone Payment Schedule tab.
Milestone Payment Summary	Not included in page count	• Schedule of proposed payments tied to completion of specific milestones.
Table of Cost Share and Contributors	Not included in page count	• Detailed breakdown of cost share amounts and contributing organizations (if applicable).
Domestic Production Plan	Not included in page count	• Strategy for ensuring domestic production capabilities and compliance with CHIPS Act requirements.
Letters of Commitment	Not included in page count	• Formal letters from all organizations providing substantive support, resources, and/or cost share.
Quad Summary	Not included in page count	• One-page visual summary of key proposal elements; must only contain information that is already present elsewhere in the proposal.
Research Security Capabilities	Not included in page count	• Overview of organizational security protocols, infrastructure, and compliance measures. Included in Research Security Packet, which is a separate attachment.
Research Security Overview	Not included in page count	• Comprehensive security plan addressing information protection, access controls, and compliance with relevant regulations. Maximum of 3 pages. Included in Research Security Packet, which is a separate attachment.
Resumes / CVs	Not included in page count	• During proposal submission, only submit for PI and at least one Co-PI for all subawardees. Maximum of 5 pages per Resume/CV. Included in Research Security Packet, which is a separate attachment.
Current and Pending Support Forms	Not included in page count	• During proposal submission, only submit for PI and one Co-PI per subawardee. Included in Research Security Packet, which is a separate attachment.

7.3 Appendix C: Project Narrative Requirements

7.3.1 Project Narrative Required Sections

C.1 ***Cover Page [Not included in page count]***

- Proposers should refer to the Cover Page Template within the Project Narrative Template document at https://natcast.org/research-and-development/smap

C.2 ***Executive Summary -*** Proposers should provide a concise summary/abstract of the proposed effort including the following information:

- Project Objectives (max. 1 paragraph summary)
- Methods to be employed
- Potential impact of the proposed project (i.e. benefits, outcomes, etc.)

C.3 ***Goals and Impact -*** Proposers should clearly describe what they are trying to achieve and the potential impact (qualitatively and quantitatively) of the work they are proposing. The Goals and Impact section must begin with a clear problem statement that demonstrates understanding of current technical challenges and market needs. Proposers should define specific, measurable project outcomes that align with the funding opportunity's goals and objectives and contribute to the specific evaluation criteria. Include preliminary data or previous relevant work that supports feasibility and validates team capabilities.

- Proposers shall articulate the broader impacts of successful project completion, including:
- benefits to the semiconductor ecosystem,
- advancement of scientific knowledge, and
- practical applications.
- Address how the proposed solution compares to existing approaches and identify technical innovations, demonstrating meaningful advancement beyond the current state of practice.

C.4 ***Management Plan -*** Proposers should provide a summary of team expertise, including any subawardees, contractors, and key personnel who will be performing work. A Principal Investigator (PI) for the project must be identified as the primary technical point of contact, along with an administrative point of contact for contractual matters.

- The management plan shall include a clear description of the team's organization, including an organization chart that shows:
    - *the programmatic relationship of team members,*

- *the unique capabilities and specialized facilities of team members,*
- *the task responsibilities of team members,*
- *the teaming strategy among the team members,*
- *and key personnel, with the level of effort (LoE) to be expended by each person during each year.*

- Proposers should explain how their team structure ensures comprehensive coverage of all technical aspects of the program and demonstrates well-organized program management.
- Additionally, proposers must detail their coordination approach, including specific guidelines for interaction among subawardees and contractors, and present a robust risk management strategy with specific mitigation approaches. The plan should confirm access to all necessary facilities and equipment required for program success. Any formal teaming agreements essential to execute the proposed research must be described.

C.5 *Technical Plan* - Proposers should outline and address technical challenges inherent in the approach and possible solutions for overcoming potential problems. This section should provide appropriate measurable milestones (quantitative if possible) at intermediate stages of the proposed research to demonstrate progress, and a plan for achieving the milestones. The technical plan should demonstrate a deep understanding of the technical challenges and present a credible (even if risky) plan to achieve the proposal's stated goal and discuss mitigation of technical risk.

- In the technical plan, the proposer may broadly outline a general approach consistent across *Phases and Tasks as* appropriate, however, each *Task Area* must be proposed and budgeted independently.
- As part of their proposal, the team should document how they plan to transition their project results to NSTC within the project narrative. This plan should include a discussion of the productivity gains for proposers, NSTC members, and others in the semiconductor ecosystem. Additionally, the plan should highlight the benefits and integration of the research for other key CHIPS programs. Furthermore, the plan should cover the transfer and maintenance of modeling software/scripts and how they can be made available to users, such as through cloud deployment, especially if such workflows depend on existing proprietary software.

C.6 *Fundamental Research Declaration* - Proposers should identify which of the proposed research activities, if any, the proposer believes should be considered as fundamental research and the rationale for that determination. For any proposed

fundamental research, proposers should identify the involved project team member(s).

C.7 ***Proposed International Collaborations -*** If an international collaboration is required for the project, proposers must provide a written justification demonstrating:

- That the foreign partner's involvement is essential to advancing program objectives, such as by offering access to unique facilities, IP, or expertise that is otherwise not readily available in the United States.
- The adequacy of any agreements and protocols between the proposer and foreign partner regarding IP protection, data protection and compliance with 4656(g).
- The partnership does not jeopardize the soundness of the project's proposed pathway to domestic production (Refer to Section 2.6).
- As applicable, the foreign partner will comply with any necessary nondisclosure agreements, security regulations, export control laws, audit requirements, and other governing statutes, regulations, and policies.
- The foreign partner is not based in a foreign country of concern as defined at 15 U.S.C. §4651(7) and implemented by the final rule entitled Preventing the Improper Use of CHIPS Act Funding, 88 FR 65600 (Sept. 25, 2023), codified at 15 C.F.R. §231.104; and 6. the foreign partner agrees to be subject to a national security review by CHIPS R&D AND workforce, which may include a risk assessment of IP leakage, if appropriate.
- For organizations with mixed domestic/foreign structure, evidence of meaningful U.S. presence through R&D facilities or production capabilities (note: sales offices alone do not constitute meaningful presence).
- Clear documentation of where work will be performed and how technical information will be protected, including:
    - Physical location of all research and development activities
    - Export control compliance measures
    - Security protocols for international data sharing
    - Monitoring procedures for international activities
- If proposing use of overseas facilities or equipment:
    - Justification for why domestic alternatives are not viable
    - Plans for transitioning to domestic capabilities when available
    - Technical information protection protocols
- For international personnel:
    - Confirmation that non-U.S. citizens working in the U.S. are lawfully present and authorized to work

- Documentation of compliance with export control requirements
- Security review compliance verification

C.8 ***Intellectual Property and Rights Management Plan*** **-** An example Intellectual Property Management Plan is included in the Project Narrative Template at: https://natcast.org/research-and-development/smap.

Each proposer must submit an Intellectual Property Management Plan (IPMP), in which the proposer should clearly identify:

- Any Background IP, that is expected to be incorporated into, embodied in or otherwise used to complete the Deliverables, and whether this Background IP is being made available to Natcast and NSTC members on a non-exclusive royalty free basis or is excluded IP.
- It is recommended that in connection with identified Background IP, proposer (i) should identify the excluded Background IP (*i.e.* pre-existing workflows, methods, system parameters, commercially available software and tools, etc.) with as much specificity as reasonably possible, describe how the excluded Background IP is used in or relates to the Deliverables, and describe how the requested exclusion for the Background IP could be expected to affect the Deliverables, the usability thereof, and achievement of the goals of the SMAP program, and (ii) should (a) specify the pricing, licensing and other commercial terms under which the performer would license the otherwise excluded Background IP to Natcast and NSTC members after the SMAP Program is over or (b) state that it is unwilling to make available or license the excluded Background IP. The reasonableness of the commercial terms for the excluded Background IP will be a criterion in evaluating the proposal.

Additionally, the Intellectual Property Management Plan should identify any encumbrances on the Deliverables or Related IP (*e.g.,* third party IP) that could affect the obligations of the performer or the rights of Natcast and NSTC members.

The IPMP may also identify any restrictions on use of the Deliverables, such as restrictions on commercial use of software by Natcast or NSTC members. For any commercial restrictions, proposer should specify the pricing, licensing and other commercial terms under which the performer would license the Deliverable for commercial use. The reasonableness of the commercial terms for any restricted Deliverable will be a criterion in evaluating the proposal. Pursuant to 15 U.S.C. § 4656(g), the proposer should describe how the proposed management and ownership of inventions that are or may be patentable will ensure domestic control

of such CHIPS funded intellectual property, including to protect such intellectual property from foreign adversaries.

Section 2.5.1 describes both the minimum required and desired IP rights for the SMAP program, and the Intellectual Property Management Plan should affirm the proposer's commitment to the minimum required IP terms. Additionally, the proposer should specify its commitment to any preferred terms (as identified in Table 4) or propose any alternative terms that align with the SMAP program goals. Terms that align with goals of the SMAP program and provide potential benefits to Natcast and NSTC members, as described in Section 5.1, will be considered as an evaluation criterion.

The proposer should also confirm that it agrees to make all workforce content, as called out in the CFP, available to Natcast under a Creative Commons Attribution (CC BY 4.0) license (https://creativecommons.org/licenses/by/4.0/). The proposer also agrees that Natcast may upload the content to NSTC's workforce repository to support workforce development efforts by Natcast and other CHIPS programs.

7.3.2 Appendices

C.9 ***Table of Abbreviations and Acronyms*** **–** An alphabetical list of all abbreviations, acronyms, and their meanings.

C.10 ***Bibliographic List of References*** **–** A complete bibliographic listing of all references used within the application.

C.11 ***Table of Subawardees (Funded Participants) and Unfunded Collaborators*** **–**

A table that identifies all organizations that will participate in and collaborate with the awarded team, known at the time of the application submission. The table should consist of an alphabetically ordered list by organization of all team members, funded and unfunded, including any known contractors.

C.12 ***Statement of Work (SOW)*** **–** Include a detailed statement of work that captures and defines all the work management aspects of your project. This should feature a more detailed breakdown aligned with the major tasks outlined in the CFP and should include, but not be limited to, key tasks and activities necessary to achieve the project objectives, research methods and experimental designs to be used, and the expected outputs, such as reports, publications, datasets, software, and prototypes. Include start and end dates for each phase or key activity. The budget workbook should align with the work breakdown structure (WBS) of the SOW through consistent task numbering and organization. Proposers must ensure that

each WBS element in the SOW corresponds directly to a budget line item using the same numerical designation (e.g., SOW Task 2.3.1 correlates to Budget Item 2.3.1).

An example SOW is available in the Project Narrative Template at: https://natcast.org/research-and-development/smap

C.13 *Budget Workbook*

- ***Budget Workbook Requirements*** - To be uploaded separately as an excel spreadsheet, using the Natcast approved Budget Workbook (BW) available at https://natcast.org/research-and-development/smap.

  Proposers must maintain the original structure of the BW template. Do not add, delete, or modify columns, rows, or tabs (except for the Milestone Payment Schedule tab). Any modifications to the template structure will prevent automated processing and may delay review of your proposal. If additional information is needed beyond what the template accommodates, please use the dedicated blue "Optional Additional Info" tab provided in the template to include explanatory text, references to supporting documentation, or other relevant details. The total proposed costs should be a sum of the total from all partners as reflected on the Cost Summary tab. Please **do not** submit separate tabs or separate BWs for separate partners. A detailed budget workbook is not required for all subawardees for the proposal. However, during contract negotiations, Natcast may request detailed information to support due diligence and finalizing the award agreement.
- ***Budget and Justification*** - Justifications for expenditures should be outlined in detail on the "Detailed Budget" tab, far right column marked "Justifications." All information must align with the amounts being requested for that individual line item and funding levels must be consistent with the project scope and allowable costs.
  - ***Direct Labor*** - The budget justification for all staff/personnel should include the following: Job title, commitment of effort on the proposed project in terms of estimated number of hours per week, and pay rate. Each labor category is intended to be matched to one job title/pay rate, which will differ for each proposal. A category may represent one or more people.
  - ***Fringe Benefits*** - Fringe benefits for each position should be identified separately from direct labor and based on rates determined by your organizational policy. The items included in the fringe benefit rate (*e.g.,*

health insurance, dental, life, FICA, etc.) This should not be charged under another cost category.

- ***Subawardees*** – Before completing this section, please see the yellow tab in the Budget Workbook template "Guide-Subawardee vs. Contractor". Each subaward should be treated as a separate item. Identify the entity, cost, and describe the scope of work to be provided by the recipient and the necessity of the subaward to the successful performance of the proposed project. A subaward is for the purpose of carrying out a portion of an Award and creates a Federal financial assistance relationship with the subrecipient.
- ***Contractors*** - Before completing this section, please see the yellow tab in the Budget Workbook template "Guide-Subawardee vs. Contractor". Each contractor or consultant should be treated as a separate item. Identify the cost (daily rate x period) or fixed fee and describe the services to be provided and the necessity of the contractors to the successful performance of the proposed project.
- ***Supplies*** - Before completing this section, please see the yellow tab in the Budget Workbook template "Federal Definitions" to differentiate between supplies and equipment. Supplies means all tangible personal property with a *per unit* cost of less than $10,000. Examples include publications, office materials, etc.
- ***Equipment*** - Before completing this section, please see the yellow tab in the Budget Workbook template "Federal Definitions" to differentiate between supplies and equipment. Equipment is defined as an item of property that has an acquisition cost of $10,000 or more and an expected service life of more than one year. The budget justification should list each piece of equipment, the cost, and a description of how it will be used and why it is necessary for the successful completion of the proposed project. Please note that any general use equipment (computers, etc.) charged directly to the award should be allocated to the award according to expected usage on the project. Natcast is required to track any equipment purchased by performer with Federal funding.
- ***Travel*** - For all travel costs, the budget justification for travel should include the destination, number of people traveling, duration, estimated transportation costs, lodging and per diem rates, and a description of how the travel is directly related to the proposed project. For travel that is yet to be determined, please provide the best

estimates based on prior experience. For budgeting purposes, a list of anticipated in-person travel locations is found in Section 1, Table 1.

- ***Other Direct Costs*** – Include less common items that do not have a specific heading within the budget template. Please list the quantity, unit, and unit cost of each item. Include an explanation of the necessity of the cost for the completion of the proposed project. Examples include less common items such as fees, printing, etc.
- ***Cost Summary –*** Formulas in this tab automatically summarize data from all other tabs. However, there are two rows that require manual entry. Those are the rows for indirect cost estimates and proposed fee, if applicable.
- ***Indirect/Overhead Rates*** - Commonly referred to as F&A, Overhead, Indirect Costs (IDC), are defined as costs incurred by the proposer organization that cannot otherwise be directly assigned or attributed to a specific project. The justification should include a cost calculation that reflects the applicable indirect cost rate.
- ***Milestone Payment Schedule*** – This tab is for listing the Milestone payment schedule spanning the entire SMAP Program. The associated tasks and subtasks in this section need to align with the SOW. Proposers must number your milestones. Proposers can add the number of milestones they like; there is no set number.
- ***Optional*–Additional Info** – This tab is to convey any additional budget information, if needed.

C.14 Milestone Payment Summary – Proposers must articulate proposed programmatic milestones tied to their use of funds. Milestones will be used to negotiate payments and payment schedules with Natcast, if selected. Proposers may include proposed milestones to stand up programs, such as an initial advance, quarterly, and final payments. Each milestone should represent significant operational achievements or deliverables (*i.e.* key technical deliverables, reports, etc.) and major performance outcomes that align with the proposed scope, as described in their application.

C.15 Table of Cost Share and Contributors – Where voluntary, committed cost share is offered, a table with details about all contributing sources of cost share, both cash and in-kind, including the rationale for selection of the contribution and the merits and risks associated with each known and anticipated contribution.

- ***Leveraged Resources –*** Proposers are not required to provide cost sharing or matching funds. Including such funds is not one of the application screening

criteria and applications that include any form of cost sharing or match will not receive additional consideration during the review process. Instead, Natcast considers any resources contributed to the project beyond the funds provided by the agency as leveraged resources. Proposers are strongly encouraged to leverage additional funds to support the project but leveraged resources are not required. Leveraged resources can come from a variety of sources, including, but not limited to, employers, industry associations, labor organizations, community-based organizations, education and training providers, philanthropic organizations, and/or state, and local government.

C.16 ***Domestic Production Plan*** - Per the guidelines in Section 2.6, proposers must explain the extent to which they plan to engage in production in the United States of any intellectual property (in the form of tangible assets), as defined for purposes of 15 U.S.C. § 4656(g), developed through this funding opportunity. For the purpose of this Call for Proposals (CFP), only activities relating to creation of tangible assets such as memory and advanced packaging technologies, but not intangible assets such as software and designs, are subject to the Department's domestic production requirements.

The Proposer must explain, at a minimum, whether and to what extent they plan to produce these tangible assets in the United States. If production is planned domestically, proposers should specify the particular vendor and the physical location (i.e., city and state), if known at the time of submission. If, however, the Proposer intends to produce any of these tangible assets outside the United States, the Proposer must provide the same location information (i.e., particular city and country and any particular vendor) and additionally explain why it is not reasonably "possible" to conduct these production activities in the United States.

A proposal's initial plans to engage in domestic production may be refined over the course of the award and must be updated on at least a yearly basis for the duration of the award. To the extent it is not reasonably "possible" for any Proposers to conduct certain covered "production" activities in the United States (15 U.S.C. § 4656(g)), the Proposers must provide their reasons, relying on the following factors:

- The availability or lack of availability of domestic production capabilities, which may consider:
    - Planned or previous efforts made to locate, develop, or contract for the production of the CHIPS R&D-funded technology, or relevant similar technologies, in the United States
    - Access to resources and other material inputs required for production

  - The expected additional product development time or cost required to make U.S. production of the CHIPS R&D-funded technology commercially feasible
  - The relative costs of domestic versus foreign production of the CHIPS R&D-funded technology, at relevant production volumes
- Commercial adoption risks and benefits, such as:
  - Risks to the market acceptance and to the value proposition for the CHIPS-funded technology, resulting from U.S. production
  - Expected commercial, economic, or national security benefits to the United States resulting from distributed production among U.S. and overseas sites
- Any other factors that are important to the success of the CHIPS R&D-funded technology

Proposers should provide sufficient detail in their Domestic Production Plans to demonstrate thoughtful consideration of these factors and a genuine commitment to maximizing domestic production where feasible.

A proposer's initial plan for domestic production may be refined over the course of the award and must be updated on at least a yearly basis for the duration of the award. These updates should reflect changing market conditions, technological developments, and production capabilities.

C.17 Letters of Commitment - Each partner organization and/or subawardee cited by the lead proposer as providing services to support the program model and lead proposer must submit a Letter of Commitment.

Letters of Commitment must address the level of participation, qualifications of the personnel who will be actively involved, and how successful completion of this project would positively impact their profession or community. Letters must be signed by an individual with authority to legally bind the organization to its commitment. Letters of Commitment must also specify any voluntary committed cost-share, including the specific services and/or products to be used in the project.

C.18 Quad Summary - Submit a Quad summary page (see separate Quad Summary Template at https://natcast.org/research-and-development/smap) that includes the following details:

- Program Overview: A high-level summary of the project, capturing the key technologies to be developed within its scope.
- Representative image or graphic: One or more image/visual relevant to the project.
- Budget High level chart or table with key budget figures and timeline
- Summary of Proposal details:
    - Team Lead
    - Team Composition
    - Focus Area(s)
    - Partnerships
    - TRL Level

The information on the quad summary page should not contain any details that are not already included in the proposal. Submit as a .pptx compatible file in landscape mode.

C.19 Research Security Packet - The following four items are to be included in the Research Security Packet and uploaded to OpenWater as a single PDF:

- ***Research Security Capabilities*** - All proposers must describe their research security capabilities and be prepared to develop or improve their research security plans if selected for an award. Proposers must provide a brief summary of proposer's current capabilities related to Research Security that addresses cybersecurity, foreign travel, research security training, and export control to protect against adversarial exfiltration. Each proposer also must attest that, if preliminarily selected for an award, the proposer has the capacity and intends to develop a Research Security Plan prior to receipt of the award demonstrating that NSTC-funded research and associated data products will be protected, by including the following statement below:

    - ***(Insert Organization Name) Research Security Capabilities***

      Does the organization have an existing research security program (Yes/No)?

      If yes, by submitting this proposal, the proposer acknowledges that depending on an assessment by Natcast in collaboration with NIST, it may be asked to improve the described program as a condition of award.

If no, by submitting this proposal, the proposer acknowledges that, if selected for award negotiation, the proposer has the capacity and intends to develop a robust Research Security Plan prior to receipt of the award demonstrating that Natcast funded research and associated IP and data products will be protected. The proposer also acknowledges that a lack of progress in implementing elements of such a plan may delay award or impact the execution of the program, potentially halting progress until the plan is fully implemented.

- ***Research Security Overview (at most 3 pages)***

  For organizations that have an existing research security program or elements of such a program, provide a written plan description that:

  - Names a point of contact on research security issues within the project leadership team;
  - Describes internal processes or procedures to address foreign talent recruitment programs, conflicts of commitment, conflicts of interest, research security training, and research integrity for application team personnel;
  - Addresses cybersecurity in the planning, design, and project oversight phases, describing measures taken to ensure that appropriate practices for cybersecurity —such as the NIST Cybersecurity Framework and Cybersecurity and Infrastructure Security Agency (CISA) Cybersecurity Performance Goals (CPGs) —are incorporated; and
  - Lists any relevant certifications in place or plans to obtain such certifications (e.g., FCL, CMMC, FedRAMP) and standards they follow (e.g. ISO/IEC 27001, ISO 8000-51, NIST 800-171).

  Proposers *may refer to the CHIPS Technology Protection Guidebook as a reference.*

- **Resumes or CVs -** Proposers must provide resumes/CVs for the Principal Investigator (PI) and all Co-Principal Investigators only. However, upon selection for award, all additional key personnel / covered individuals identified in the proposal will be required to submit their resumes/CVs as part of the pre-award documentation process.

The following formats are acceptable Research Security resume/CV documentation:

- NSF-format biosketches exported from SciENcv are preferred with ORCID #, if available.
- Traditional academic CVs and institutional standardized biographies are acceptable (maximum 5 pages).
- All formats must include, at minimum:
  - Name
  - ORCID # (if available)
  - Contact information (email, phone, address)
  - Current organization
  - Educational background
  - Work history (past 5 years)
  - Relevant accomplishments
  - Current organizational affiliations.

- **Current and Pending Support Forms (CPSF) -** Each PI and at least one Co-PI from each subawardee must enumerate current and pending support information for all federally funded research projects. Only the PI and a Co-PI from each listed sub-awardee must submit their CPSF during the proposal phase. The CPSF information may be submitted to Natcast by:

  - Exporting the CPSF from the NSF SCV system and attaching it to the proposal after the PI/Co-PI's CV/resume or
  - Using the online form available at: https://forms.office.com/g/HscpN1n8Wz.
    - If utilizing the second method, the online form requires the proposal application number and title to match those in the online submission portal at https://natcast.secure-platform.com/rnd/organizations/main/home

If a proposal is selected by Natcast, the proposer will be required to submit a list of all covered individuals during award stage negotiations. A covered individual is defined as a person who contributes in a substantive, meaningful way to the scientific development or execution of a research and development project proposed. Note that NIST generally does not consider individuals who only conduct isolated tasks incidental to the research (for example, setting up equipment or performing administrative functions) or individuals who support research by executing discrete tasks as directed as

covered individuals. Consistent with guidance for implementing NSPM-33, disclosures from broader classes of individuals (e.g., certain graduate students and undergraduate students) will generally be unnecessary, except when the activities of such an individual in a specific proposal rise to the level of meeting the definition of a "covered individual" under 42 U.S.C. § 6605(d)(1). For instance, NIST views authorship of a technical or scholarly publication as evidence of a truly substantial professional contribution to the research, given an author's participation in conceiving or evolving the project design, executing one or more significant aspects of the project, or documenting the project results in a form accessible to the scientific community.

During proposal submission, only the Principal Investigator (PI) and at least one Co-Principal Investigator (Co-PI) from each subawardee are required to submit resumes/CVs and CPSFs. After proposal selection but before final award approval, all covered individuals identified in the proposal will be required to submit their resume/CVs and CPSFs for a research security review prior to their approval by Natcast.

7.4 Appendix D: Reference Items for Program Delivery

7.4.1 D.1 - General Program Deliverable Details

Table 10. General Program Deliverables for SMAP, description, and target schedule.

ID	Title	Description	Target Schedule
R1	Monthly Status Report (MSR)	Submit MSR in the form of a Microsoft (MS) Word document to identify key accomplishments and issues. Includes documentation supporting any new equipment purchase and/or cost sharing.	Submitted no later than 1 month from project award; monthly thereafter.
R2	Monthly Project Team Meeting	Project Team meetings with all Project Team members to discuss details of any efforts and processes executed in support of this project.	First meeting considered the Kick-Off, will be held no later than 1 month from project award; monthly project teams thereafter. Minutes submitted no later than 7 days after meeting. May be captured in the MSR.
R3	Quarterly Progress Report	Submit Quarterly Progress Report in the form of an MS Word document, Quad Chart, and briefing (slide deck) to identify key accomplishments in the reporting period, metrics, and milestones achieved. Include a description of newly developed IP, including patentable inventions, software and research results, as well as any utilization activities of such IP. Project Team member representatives must meet with assigned Natcast personnel for milestone progress updates. Project continuation/termination decisions will be made by Natcast quarterly.	Quarterly Progress Report, Quad Chart, and briefing must be submitted no later than 4 months from project award; submit quarterly thereafter.
R4	Quarterly Reviews	Natcast technical review.	First review conducted no later than 4 months from project award; conduct reviews quarterly thereafter. Reviews must be conducted within 14 days of receiving Quarterly Progress Report.

R5	Final Project Report	Detailed description of project outcomes and findings, intellectual merit and broader impacts, list of publications and outputs, impact analysis, lessons learned and recommendations transition plans and commercialization deliverable research byproducts.	Due to the end of project.
R6	Metrics Collection Plan	An intentional metrics collection plan with methodologies and a schedule that is specific to showing progress in advancing the TRL/MRLs of the project. Metrics must include Go/No-Go metrics.	Submit first plan no later than 2 months from project award; Submit revised plans annually thereafter.
Program Management (PM)			
PM1	Detailed Schedule	Schedules shall be provided for planning, statusing, controlling, modeling and specifying work activities throughout the project life cycle.	Submitted no later than 2 months from project award; monthly thereafter. May be included in the MSR.
Research Security (RS)			
RS1	Research Security Plan	Performers must submit a detailed description of their Research Security Plan which includes cybersecurity, foreign travel, research security training, and export control.	Within 20 business days of execution of the Award, submit to Natcast for approval a timeline with milestones for implementation Research Security Plan. The plan must be implemented no later than 180 days of execution of the Award; plan is updated annually thereafter.
RS2	Covered Individual List	List of all individuals in support of the program updated as needed. Personnel change notifications are required, including submission of resumes/CV and Current and Pending support form for new personnel to ensure Research Security plan compliance.	Initial list due at contract award and updated periodically as needed. Natcast Research Security to provide status update on new individuals within 14 Days of receiving updates.
RS3	Covered Individual Request	All covered individuals must enumerate current and pending support. The Covered Individual Request consists of a completed Natcast Current and Pending Support form for Covered Individual* and CV/Resume.	**Initial Covered Individuals Request are due at least 14 days prior to contract award** and must be submitted as needed (anytime a new covered individual is added to the project or

		Submit via email to researchsecurity@natcast.org. Personnel change notifications are required, including submission of a Covered Individual Request for new personnel to ensure Research Security plan compliance.	relevant information about an individual changes). Covered Individuals must have approval prior to starting work on the project. Performer must submit new covered individuals to Natcast for a research security review before the new covered individual can start working on the research project. Natcast will review the covered individual information and provide a response to the PI within 14 calendar days on whether or not Natcast approves the covered individual's involvement in the project.
Documentation (DO)			
DO2	NSTC Transition Plan	Transition plan defining how results of research can be utilized by NSTC membership. This includes a domestic production plan detailing the extent to which test vehicles can be produced domestically.	Submitted as developed during the project and included with Final Project Report.
DO3	Developed Curriculum	All relevant course material and documentation for use by NSTC membership.	Submitted as it is developed during project, and no later than end of project.

7.4.2 D.2 - Illustrative Technical Report Template

This is an example of a report needed during Program delivery for budgeting and planning purposes.

Outcomes

- **Major Goals and Objectives**
  - Accomplishments in the current period
  - Plans for the next reporting period

Outputs

- **Publications, Conference Papers, and Presentations**
  - List any publications, conference papers, and presentations produced during the reporting period.
- **Website(s) or Other Internet Site(s)**
  - Provide details of any websites or other internet sites developed as part of the project.
- **Technologies or Techniques**
  - Describe any new technologies or techniques that were developed.
- **Inventions, Patent or Copyright Applications, and/or Licenses**
  - List any inventions, patent or copyright applications, and/or licenses that resulted from the project.
- **Other Products**
  - Detail any other products such as data or databases, physical collections, audio or video products, software, models, educational aids or curricula, instruments or equipment, research material, interventions (e.g., clinical or educational), government ratification (*e.g.,* NIST, EPA, etc. for new analytical methods), or new business creation.

Risks and Changes

- **Risks and Risk Mitigation**
  - Maintain and provide a running list of significant uncertainties and their perceived impact on the project. Consider a risk matrix covering technical, managerial, and other uncertainties (*i.e.* market or external dependencies) versus impact on the project outcome (*i.e.* low, medium, high impact) depending on resolution. As progress is made, new risks or uncertainties may appear, and others may be resolved.
  - If not already accounted for in the project plan, identify any actual or anticipated problems or delays and the actions or plans to resolve them.

- **Changes in Approach**
  - Describe any changes in approach to mitigate newly discovered risks or problems and the reasons for these changes.
- **Impact on Expenditures and Timeline**
  - Discuss any changes that have a significant impact on the timeline or budget and expenditures and the reason.
  - Include documentation supporting any equipment purchased during the month (description, amount, vendor).
  - Include documentation demonstrating any cost sharing that occurred during the month.

Schedule

Capture a high-level schedule that is aligned to the SOW, documenting progress against the baseline plan.

Actuals versus Forecast

Capture spend-to-date against the baseline budget for the cost of work completed. While there is no requirement for an earned value management system, it is expected that the performer maintains some level of internal control over the budgeted work, monitors performance against it, and describes any variances from the plan.

7.4.3 D.3 - Illustrative Final Report Template

This is an example of a report needed during Program delivery for budgeting and planning purposes.

Required Sections

- **Introduction** - Overview of the project and its objectives
- **Project Outcomes or Findings** - Detailed description of the project's outcomes or findings, intellectual merit, and broader impacts
- **Publications and Outputs** - List of publications, patents, copyrights, presentation, articles, or disclosures of research results
- **Impact Analysis** - Comparison of the project's impact to the expected outcomes
- **Lessons Learned and Future Recommendations** - Insights and recommendations for future NSTC R&D Programs
- **Transition Plans and Commercialization** - Discuss how to advance the economic goals of the NSTC
- **Deliverables and Research Byproducts** - Descriptions, instructions, and artifacts associated with project deliverables and research byproducts, potentially including but not limited to:

  - Datasets
  - Source code
  - Object code
  - Curriculum and labs
  - Copyrighted materials
- **Expected Publication of Results** - Information on the expected publications of results and other relevant details for NSTC members
- **Citations and Links** - Citations and links to publicly accessible data and other public outputs