Request for Information (RFI)

Co-packaged Optical Engine Development for AI Infrastructure Scale-up

Issued: July 1, 2025

Deadline for submissions: July 29, 2025

Overview: Natcast, the operator for the CHIPS for America National Semiconductor Technology Center (NSTC), is seeking public input on a potential research program on co-packaged optical engine development.

Background: The rapid expansion of AI models and workloads is outpacing the capabilities of traditional electrical interconnects. This program aims to integrate optical transceivers directly into physical packages to reduce power consumption, improve signal integrity, and enhance bandwidth density for AI and high-performance computing (HPC) infrastructure scale-up.

Objective: This RFI seeks input from stakeholders to set R&D priorities for co-packaged optical engines aimed at scaling AI and HPC infrastructure. We invite industry, academia, and research partners to identify gaps in standards, challenges in prototyping, and barriers to commercialization. We also seek suggestions on how NSTC can foster collaboration in design, integration, co-development, and technology transfer.

Who should respond: This RFI seeks inputs from a broad range of organizations that may benefit from such a research program: foundries, outsourced semiconductor assembly and test (OSATs), integrated device manufacturers (IDMs), fabless semiconductor companies, end users, materials suppliers, equipment vendors, academia, startup companies, small businesses, technology incubators, government labs, federally funded research and development centers (FFRDCs), university applied research centers (UARCs), the defense industrial base, and other commercial semiconductor companies and cloud service providers (CSPs).

Disclaimer: This RFI is not a solicitation for concept papers or proposals, but an information-gathering effort to shape effective, impactful next steps. Any costs incurred by interested parties in response to this announcement will not be reimbursed. Respondents acknowledge that by participating in this RFI, they grant Natcast permission to use the contact details provided in the response for direct communication concerning this RFI and any subsequent collaborations.

Instructions:

- Responses must be entered into the RFI response template provided. Submissions that do not follow the template will not be reviewed.

- References, figures, acronym tables should be appended at the end of the template with each figure clearly indicating the corresponding question number. The final submission must be in PDF format.
- Please clearly mark confidential business information or other nonpublic information in your response. Be advised that Natcast may share a summary of aggregated response data with the Department of Commerce and/or other third parties, including potential release to the public. This summary will not include respondents' individual submissions, or any confidential or identifying information. By submitting your response, you consent that information from your response may be aggregated as part of that summary.
- Responses must be submitted no later than 5 PM EDT on July 29, 2025.

Please upload your RFI response to http://www.natcast.org/rfi.

Submit any questions to research@natcast.org.

RFI Questions and Discussion Topics

1. Background
    a. Submissions should include the following information:
        i. Organization name
        ii. Size of organization in either revenue or employees, as appropriate
        iii. Name and title of primary point of contact
        iv. Email of the primary point of contact
    b. Briefly describe your current organization in a paragraph. Feel free to include web links for further information. Do not include large corporate overview presentations.
    c. Have you participated in, or do you plan to participate in other CHIPS Act programs?
    d. Describe your prior and current interests and work in co-packaged optics (CPO) for advanced AI Infrastructure applications and provide examples including, but not limited to, publications, presentations, patents, etc.
2. Technical Performance and Roadmap
    a. What system architectures should be explored that incorporate hybrid electrical-optical processing and communications technologies?
    b. What key performance indicators (KPIs), e.g. bandwidth density, energy efficiency, latency, etc., should co-packaged optical engines hit by 2030 and 2035 to stay ahead of projected AI demand? What top two areas have the highest risk/reward for advancing end system KPIs?
    c. Which optical I/O technologies and light sources (e.g., comb lasers, QD lasers, VCSEL, micro-LED, etc.) are promising for scalable deployment?

   d. How should optical connectors and cables evolve to support high-density, cost-effective deployment?

3. Standards, Interfaces, and Interoperability
   a. Do existing standard bodies address the needs for CPO engine development sufficiently? Please cite specific gaps and areas NSTC can enable improvements.
   b. What level of standardization would be most helpful for facilitating broader innovation in photonic integrated circuit (PIC) to electronic integrated circuit (EIC) integration?
   c. What are the bottlenecks in PIC, EIC and PIC-to-EIC co-design, fabrication, assembly, test, and integration?
   d. Rank the importance of electrical, optical, mechanical, and thermal interface specs for first-generation deployment.
   e. What process or packaging standards would best enable scalable and cost-effective wafer-scale manufacturing for CPO?
   f. How should energy consumption per bit be defined and measured to ensure consistent benchmarking?
4. Prototyping, Test, & Metrology
   a. What are the most critical manufacturing challenges currently hindering the high-volume cost-effective production of CPO modules (e.g. fiber to PIC alignment, thermal management, optical testing, heterogeneous integration, etc.)?
   b. What are the critical process modules currently lacking high-volume manufacturing (HVM) capacity?
   c. Which key materials systems and substrates are most critical and require improved access for R&D?
   d. What test capabilities should be prioritized for R&D?
   e. What metrology capabilities should be prioritized the most for R&D?
   f. What are the key reliability gaps when moving from lab to fab?
5. Collaboration Mechanisms & Ecosystem Development
   a. Where is the most suitable place to conduct this research and what capabilities are currently missing?
   b. Which shared assets should NSTC prioritize – such as multi-project PIC shuttles, a neutral photonics process development kit (PDK), open reference designs, or a pilot packaging line?
   c. How can a manufacturing ecosystem be structured to facilitate collaboration among foundries, OSATs, and system integrators?

   d. What actions would most effectively support ecosystem development, such as open access to foundry flows, shared packaging infrastructure, and modular "Lego block" components?
6. To advance domestic optical interconnect technology, which is more critical: enablement infrastructure, targeted research funding, or a combination of both? Please elaborate with specifics.
7. Considering previous research initiatives such as DARPA PIPES, NSF's Research on Integrated Photonics Utilizing AIM Photonics, what opportunities exist to extend or build upon these funded R&D programs?
8. What role should NSTC play in driving standards, access, and investment for CPO, and how can your organization contribute?
9. Please suggest anything else that we should consider formulating this potential research program

Please attach any references, figures, tables of acronyms on final page of the template.