**Request for Information (RFI)**

Co-packaged Optical Engine Development for AI Infrastructure Scale-up

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| --- | --- |
| **1** | **Background** |
|  |  Organization Name | Click or tap here to enter text. |
|  |  Type of Organization | Choose an item. |
|  |  Number of Employees | Click or tap here to enter text. |
|  |  Annual Revenue ($) | Click or tap here to enter text. |
|  |  Primary Contact Name | Click or tap here to enter text. |
|  |  Primary Contact Email | Click or tap here to enter text. |
|  |  |
| 1a | Briefly describe your current organization in a paragraph. Feel free to include web links for further information. |
|  | Click or tap here to enter text. |
| 1b | Have you participated in, or do you plan to participate in other CHIPS Act programs? |
|  | Click or tap here to enter text. |
| 1c | Describe your prior and current interests and work in co-packaged optics (CPO) for advanced AI Infrastructure applications and provide examples including, but not limited to, publications, presentations, patents, etc. |
|  | Click or tap here to enter text. |
|  |  |
| **2** | **Technical Performance and Roadmap** |
| 2a | What system architecture should be explored that incorporates hybrid electrical-optical processing and communications technologies? |
|  | Click or tap here to enter text. |
| 2b | What key performance indicators (KPIs), e.g. bandwidth density, energy efficiency, latency, etc., should co-packaged optical engines hit by 2030 and 2035 to stay ahead of projected AI demand? What top two areas have the highest risk/reward for advancing end system KPIs? |
|  | Click or tap here to enter text. |
| 2c | Which optical I/O technologies and light sources (e.g., comb lasers, QD lasers, VCSEL, micro-LED, etc.) are promising for scalable deployment? |
|  | Click or tap here to enter text. |
| 2d | How should optical connectors and cables evolve to support high-density, cost-effective deployment? |
|  | Click or tap here to enter text. |
|  |  |
| **3.** | **Standards, Interfaces, and Interoperability** |
| 3a | Do existing standard bodies address the needs for CPO engine development sufficiently? Please cite specific gaps and areas NSTC can enable improvements. |
|  | Click or tap here to enter text. |
| 3b | What level of standardization would be most helpful for facilitating broader innovation in photonic integrated circuit (PIC) to electronic integrated circuit (EIC) integration? |
|  | Click or tap here to enter text. |
| 3c | What are the bottlenecks in PIC, EIC and PIC-to-EIC co-design, fabrication, assembly, test, and integration?  |
|  | Click or tap here to enter text. |
| 3d | Rank the importance of electrical, optical, mechanical, and thermal interface specs for first-generation deployment. |
|  | Click or tap here to enter text. |
| 3e | What process or packaging standards would best enable scalable and cost-effective wafer-scale manufacturing for CPO? |
|  | Click or tap here to enter text. |
| 3f | How should energy consumption per bit be defined and measured to ensure consistent benchmarking? |
|  | Click or tap here to enter text. |
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| **4.** | **Prototyping, Test, & Metrology** |
| 4a | What are the most critical manufacturing challenges currently hindering the high-volume cost-effective production of CPO modules (e.g. fiber to PIC alignment, thermal management, optical testing, heterogeneous integration, etc)? |
|  | Click or tap here to enter text. |
| 4b | What are the critical process modules currently lacking high-volume manufacturing (HVM) capacity? |
|  | Click or tap here to enter text. |
| 4c | Which key materials systems and substrates are most critical and require improved access for R&D? |
|  | Click or tap here to enter text. |
| 4d | What test capabilities should be prioritized for R&D? |
|  | Click or tap here to enter text. |
| 4e | What metrology capabilities should be prioritized the most for R&D?  |
|  | Click or tap here to enter text. |
| 4f | What are the key reliability gaps when moving from lab to fab? |
|  | Click or tap here to enter text. |
|  |  |
| **5** | **Collaboration Mechanisms & Ecosystem Development** |
| 5a | Where is the most suitable place to conduct this research and what capabilities are currently missing? |
|  | Click or tap here to enter text. |
| 5b | Which shared assets should NSTC prioritize – such as multi-project PIC shuttles, a neutral photonics process development kit (PDK), open reference designs, or a pilot packaging line? |
|  | Click or tap here to enter text. |
| 5c | How can a manufacturing ecosystem be structured to facilitate collaboration among foundries, OSATs, and system integrators?  |
|  | Click or tap here to enter text. |
| 5d | What actions would most effectively support ecosystem development, such as open access to foundry flows, shared packaging infrastructure, and modular “Lego block” components? |
|  | Click or tap here to enter text. |
|  |  |
| **6** | **To advance domestic optical interconnect technology, which is more critical: enablement infrastructure, targeted research funding, or a combination of both? Please elaborate with specifics.** |
|  | Click or tap here to enter text. |
|  |  |
| **7** | **Considering previous research initiatives such as DARPA PIPES, NSF’s Research on Integrated Photonics Utilizing AIM Photonics, what opportunities exist to extend or build upon these funded R&D programs?** |
|  | Click or tap here to enter text. |
|  |  |
| **8** | **What role should NSTC play in driving standards, access, and investment for CPO, and how can your organization contribute?**  |
|  | Click or tap here to enter text. |
|  |  |
| **9** | **Please suggest anything else that we should consider formulating this potential research program.** |
|  | Click or tap here to enter text. |

**Please attach any references, figures, tables of acronyms on final page of the form.**

Click or tap here to enter text.



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