Request for Information (RFI)

Interconnect Materials and Integrated Processes for Power-Performance-Area (PPA) Improvement in Compute Applications

Issued: July 10, 2025

Deadline for submissions: August 1, 2025

Overview: Natcast, the operator for the CHIPS for America National Semiconductor Technology Center (NSTC), is seeking public input on the focus and prioritization of a potential research program investigating the use of novel interconnect materials and integrated processes for Power-Performance-Area (PPA) improvement in future devices to support AI computing requirements. This program aims to bridge the lab-to-fab gap of monolithically integrated backend of line (BEOL) interconnects.

Background: The historical gains in power and performance associated with transistor density improvements are increasingly counterbalanced by heightened resistance (R) and capacitance (C) resulting from tighter pitches within the BEOL interconnects, as well as challenges in heat dissipation. As copper approaches its tipping point for both resistance and reliability with shrinking dimensions, the field has significantly focused on the use of subtractive ruthenium as an alternative to copper, among other metals. Challenges with this vector include transitioning process flows from damascene to subtractive, patterning/etching metals, and raw material cost. Overall, candidate replacement metals are evolutionary, not providing new fundamental physics to leverage.

To circumvent capacitance hurdles, researchers have been drawn to air gaps for isolating interconnects. This severely limits heat dissipation. Thus, investigating alternative low-k interlayer dielectric (ILD) materials is also merited. Current state-of-the-art utilizes variants of SiO_2, such as SiCOH, with k ~ 1.5 and thermal conductivity, κ, ~ 0.6 W/m-K. The desire is to have candidate materials that approach k = 1 with κ > 1.5 W/m-K and have a feasible path to processing below 400°C.

Objective: The primary objective of this RFI is to gather insights and recommendations from a broad range of stakeholders to help shape the R&D roadmap for the on-die BEOL interconnects NSTC research program. Natcast invites industry, academia, and research partners to identify gaps in standards and challenges in prototyping to transition from proof-of-concept demonstrations in the lab to reliable and scalable manufacturing solutions. Innovations related to die/wafer bonding will be covered in separate programs. This RFI targets three main areas:

1. Novel conducting materials for on-die interconnects (e.g.- topological semimetals, MAX[1] ceramics), excluding carbon nanomaterials as those were encompassed in a prior RFI.
2. Low-*k* ILD with high thermal conductivity (e.g.- porous matter such as low-dimensional COF[2] polymers).
3. Integrated process approaches and others that do not fall under categories 1 and 2 above (e.g.- alternative patterning options such as subtractive conductor patterning or directed self-assembly, combined barrier/liner/metallization schemes, self-forming barrier or selective thin film deposition processes that allow reducing barrier thickness).

Submitters can address one or more of the three topics.

Who should respond: This RFI seeks input from a broad range of organizations that may benefit from such a research program. This includes foundries, IDMs, materials suppliers, equipment vendors, academia, startup companies, small businesses, technology incubators, government labs, federally funded research and development centers (FFRDCs), university applied research centers (UARCs), the defense industrial base, and other commercial semiconductor companies.

Disclaimer: This RFI is not a solicitation for concept papers or proposals, but an information-gathering effort to shape effective, impactful next steps. Any costs incurred by interested parties in response to this announcement will not be reimbursed. Respondents acknowledge that by participating in this RFI, they grant Natcast permission to use the contact details provided in the response for direct communication concerning this RFI and any subsequent collaborations.

Instructions:

- Responses must be entered into the RFI response template provided. Submissions that do not follow the template will not be reviewed.
- References, figures, acronym tables should be appended at the end of the template with each figure clearly indicating the corresponding question number. The final submission must be in PDF format.
- Please clearly mark confidential business information or other nonpublic information in your response. Be advised that Natcast may share a summary of aggregated response data with the Department of Commerce and/or other third parties, including potential release to the public. This summary will not include respondents' individual submissions, or any confidential or identifying information. By submitting your response, you consent that information from your response may be aggregated as part of that summary.
- Responses must be submitted no later than 5 PM EDT on August 1, 2025.

Please upload your RFI response to: https://natcast.secure-platform.com/rnd

Submit any questions to research@natcast.org.

RFI Questions and Discussion Topics

1. Background
    a. Submissions should include the following information:
        i. Organization name
        ii. Size of organization in either revenue or employees, as appropriate
        iii. Title of primary point of contact
        iv. Email of the primary point of contact
    b. Briefly describe your current organization in a paragraph. Feel free to include a web link for further information. Do not include large corporate overview presentations.
    c. Have you participated in, or do you plan to participate in other CHIPS Act programs?
    d. Describe your prior and current interests and work in BEOL interconnects/related materials and provide examples including, but not limited to, publications, presentations, patents, etc.
2. Technical Performance and Roadmap
    a. Please indicate if your responses address area 1, 2, or 3 of this RFI. You may specify more than one area.
    b. What are the most critical challenges of local interconnect materials and processes for future logic nodes such as complementary field-effect transistors (CFET)? What are the best metrics for evaluating or quantifying benefits of a proposed research topic?
    c. Which conductor/insulator materials should be prioritized based on their potential for PPA improvement and their readiness for integration into semiconductor manufacturing processes?
    d. Based on your experience, what is the time horizon for integrating new materials into a competitive transistor node (with demonstrated comparable/superior electrical performance to copper/ruthenium or SiO_x derivatives) which enables scaling to CFET and beyond? Please be specific about which materials.
    e. What are the most promising methods for synthesizing, depositing, patterning and overall integration of candidate materials at wafer scale (200 mm or 300 mm)?

f. What key performance indicators (KPIs), e.g., RC, reliability, defect, yield, thermals etc., should BEOL interconnects achieve by 2030 and 2035 to stay ahead of projected demand?

3. Challenges and Opportunities

   a. What are the key opportunities for accelerating this timeline *via* NSTC R&D funding? Note that NSTC R&D funding can extend to shared use infrastructure, with examples such as the EUV Accelerator, the Design Enablement Gateway, or the Test Vehicle Innovation Pipeline.
   b. What are the biggest challenges for new materials integration into future transistor nodes (e.g.- ability to synthesize, deposit, or pattern, surface roughness, passivation layers, barriers, seeds, liners). Please highlight specific challenges for specific materials and processes. Mention any peripheral challenges such as modeling, benchmarking, metrology, characterization and test vehicle availability.
   c. What are the biggest challenges for interconnect materials and process candidates to scale from coupon to 200 or 300mm? Examples of challenges include:
      i. Limitations of synthesis or deposition processes when dealing with 200 or 300 mm wafers
      ii. Physical characterization in either the laboratory or inline
      iii. Thermal processing limitations (back-end-of-line processes require <400^{o}C)
      iv. Patterning to prove device characteristics at sub-2nm logic node
      v. Device characterization including statistical variation and reliability (line mean time to fail, ILD time-dependent dielectric breakdown)
      vi. Materials compatibility (e.g.- deposition methods that do not damage vias, intermixing due to diffusion)

4. Collaboration Mechanisms & Ecosystem Development

   a. Beyond the technical challenges, what are the logistical, institutional, and organizational challenges involved in transitioning candidate materials from laboratory research to commercial production? For example, is there enough raw material in existence that supply chains can utilize to meet potential demands?
   b. Where is the most suitable place to conduct this research and what capabilities are currently missing?
   c. What previous research programs exist that can be a starting point, and what opportunities are there to extend or build upon these funded R&D programs?

   d. For an organization such as yours, what type of partnerships and research funding would be required to form a holistic research effort on interconnect materials directly translating to an industrially relevant prototype?
   e. Which shared assets should NSTC prioritize – such as process tools, patterned vehicle availability, metrology, testing, etc.?
5. Please suggest anything else that we should consider when formulating this research program.