**Request for Information (RFI)**

Interconnect Materials and Integrated Processes for Power-Performance-Area (PPA) Improvement in Compute Applications

|  |  |  |
| --- | --- | --- |
| **1.** | **Background** | |
|  | Organization Name | Click or tap here to enter text. |
|  | Type of Organization | Choose an item. |
|  | Number of Employees | Click or tap here to enter text. |
|  | Annual Revenue ($) | Click or tap here to enter text. |
|  | Primary Contact Name | Click or tap here to enter text. |
|  | Primary Contact Email | Click or tap here to enter text. |
|  |  | |
| 1a | Briefly describe your current organization in a paragraph. Feel free to include web links for further information. | |
|  | Click or tap here to enter text. | |
| 1b | Have you participated in, or do you plan to participate in other CHIPS Act programs? | |
|  | Click or tap here to enter text. | |
| 1c | Describe your prior and current interests and work in co-packaged optics (CPO) for advanced AI Infrastructure applications and provide examples including, but not limited to, publications, presentations, patents, etc. | |
|  | Click or tap here to enter text. | |
|  |  | |
| **2.** | **Technical Performance and Roadmap** | |
| 2a | Please indicate if your responses address area 1, 2, or 3 of this RFI. You may specify more than one area. | |
|  | Click or tap here to enter text. | |
| 2b | What are the most critical challenges of local interconnect materials and processes for future logic nodes such as complementary field-effect transistors (CFET)? What are the best metrics for evaluating or quantifying benefits of a proposed research topic? | |
|  | Click or tap here to enter text. | |
| 2c | Which conductor/insulator materials should be prioritized based on their potential for PPA improvement and their readiness for integration into semiconductor manufacturing processes? | |
|  | Click or tap here to enter text. | |
| 2d | Based on your experience, what is the time horizon for integrating new materials into a competitive transistor node (with demonstrated comparable/superior electrical performance to copper/ruthenium or SiOx derivatives) which enables scaling to CFET and beyond? Please be specific about which materials. | |
|  | Click or tap here to enter text. | |
| 2e | What are the most promising methods for synthesizing, depositing, patterning and overall integration of candidate materials at wafer scale (200 mm or 300 mm)? | |
|  | Click or tap here to enter text. | |
| 2f | What key performance indicators (KPIs), e.g. RC, reliability, defect, yield, thermals etc., should BEOL interconnects achieve by 2030 and 2035 to stay ahead of projected demand? | |
|  | Click or tap here to enter text. | |
|  |  | |
| **3.** | **Challenges and Opportunities** | |
| 3a | What are the key opportunities for accelerating this timeline *via* NSTC R&D funding? Note that NSTC R&D funding can extend to shared use infrastructure, with examples such as the [EUV Accelerator](https://natcast.org/facilities/euv), the [Design Enablement Gateway](https://natcast.org/facilities), or the [Test Vehicle Innovation Pipeline](https://natcast.org/research-and-development/tvip). | |
|  | Click or tap here to enter text. | |
| 3b | What are the biggest challenges for new materials integration into future transistor nodes (e.g.- ability to synthesize, deposit, or pattern, surface roughness, passivation layers, barriers, seeds, liners). Please highlight specific challenges for specific materials and processes. Mention any peripheral challenges such as modeling, benchmarking, metrology, characterization and test vehicle availability. | |
|  | Click or tap here to enter text. | |
| 3c | What are the biggest challenges for interconnect materials and process candidates to scale from coupon to 200 or 300mm? Examples of challenges include:   1. Limitations of synthesis or deposition processes when dealing with 200 or 300 mm wafers 2. Physical characterization in either the laboratory or inline 3. Thermal processing limitations (back-end-of-line processes require <400oC) 4. Patterning to prove device characteristics at sub-2nm logic node 5. Device characterization including statistical variation and reliability (line mean time to fail, ILD time-dependent dielectric breakdown) 6. Materials compatibility (e.g.- deposition methods that do not damage vias, intermixing due to diffusion) | |
|  | Click or tap here to enter text. | |
|  |  | |
| **4.** | **Collaboration Mechanisms & Ecosystem Development** | |
| 4a | Beyond the technical challenges, what are the logistical, institutional, and organizational challenges involved in transitioning candidate materials from laboratory research to commercial production? For example, is there enough raw material in existence that supply chains can utilize to meet potential demands? | |
|  | Click or tap here to enter text. | |
| 4b | Where is the most suitable place to conduct this research and what capabilities are currently missing? | |
|  | Click or tap here to enter text. | |
| 4c | What previous research programs exist that can be a starting point, and what opportunities are there to extend or build upon these funded R&D programs? | |
|  | Click or tap here to enter text. | |
| 4d | For an organization such as yours, what type of partnerships and research funding would be required to form a holistic research effort on interconnect materials directly translating to an industrially relevant prototype? | |
|  | Click or tap here to enter text. | |
| 4e | Which shared assets should NSTC prioritize – such as process tools, patterned vehicle availability, metrology, testing…etc.? | |
|  | Click or tap here to enter text. | |
|  |  | |
| **5.** | Please suggest anything else that we should consider when formulating this research program. | |
|  | Click or tap here to enter text. | |
|  |  | |

**Please attach any references, figures, tables of acronyms on final page of the form.**

Click or tap here to enter text.



**Disclaimer:** This RFI is not a solicitation for concept papers or proposals, but an information-gathering effort to shape effective, impactful next steps. Any costs incurred by interested parties in response to this announcement will not be reimbursed. Respondents acknowledge that by participating in this RFI, they grant Natcast permission to use the contact details provided in the response for direct communication concerning this RFI and any subsequent collaborations.