Policy Memo:
Alignment of the NSTC and White House AI and U.S. Semiconductor Priorities

August 19, 2025

1. Executive Summary

The National Semiconductor Technology Center (NSTC) is aligned closely with the priorities of the Trump Administration as highlighted in the recently released White House AI Action Plan, the Restoring Gold Standard Science Executive Order, and through high-risk, high-reward, leap-ahead R&D. Through addressing the challenges posed by the rapid advancements in global semiconductor capabilities, the NSTC is a linchpin to realize a more prosperous, competitive, and secure leadership position for the United States' continued dominance in semiconductor technologies.

Before Congress authorized the NSTC, U.S. semiconductor researchers, startups, and companies were significantly underserved by the R&D and facilities resources in the United States. While much of the R&D infrastructure, such as the DOE, was engaged in excellent basic R&D, semiconductor research and resources were flat-funded and siloed across agencies[1], and as they moved further along the pipeline, many were required to move their semiconductor R&D to Belgium, Taiwan, or Korea and faced long waits for prototyping and high fees. Because the U.S. lacked a robust network of semiconductor-specific research, development, and prototyping facilities, as well as coordination for advanced semiconductor development, semiconductor R&D was offshored to the EU, China, Taiwan, Korea and Japan[2], resulting in a measurable decline in patent filings in critical semiconductor areas.

[1] "Sparking Innovation: How Federal Investment in Semiconductor R&D Spurs U.S. Economic Growth and Job Creation. Report Addendum." Nathan and Associates, Semiconductor Industry Association. 05/2020.
[2] "The Next China Shock," New York Times. 07/14/25, Dr. David Autor, Dr. Robert Hansen.

Further, semiconductor industry analysts forecasted a shortage of 36,000 workers by 2030[3], and U.S. venture capital investments in semiconductors have also suffered significant outflows. In 2008, 4.3% of all VC dollars went into semiconductors ($1.6B out of $37.1B), and it has trended down since then. Despite the overall importance of the semiconductor industry, an average of less than 1.5% of all VC dollars have gone into semiconductors annually since 2015, including only 1.2% in 2022 ($2.8B of $240.9B invested across all sectors).[4]

Due to the urgency of the U.S. national weaknesses in semiconductor R&D deployment, workforce, and venture capital funding, the NSTC was uniquely designed to create a fast-moving and flexible public private consortium with all the resources of a public R&D entity, but all the advantages and speed of a private sector entity. Consequently, in its first year of operation, the consortium has moved at lightning-fast speed, engaging the U.S. semiconductor ecosystem at large, and encountering minimal obstacles in its progress. The NSTC's comprehensive approach includes developing key facilities and R&D projects, all strategically located to maximize collaboration between academia, industry, and government. This rapid advancement is underpinned by a strategic plan that prioritizes extending U.S. semiconductor leadership, reducing the time and cost to prototype, and building a robust U.S. workforce ecosystem.

As the Trump Administration moves quickly to ensure U.S. technology dominance, the NSTC is playing a critical role in advancing U.S. leadership in the foundational technologies – semiconductors – that are driving the technological breakthroughs and applications of the future.

2. White House AI Action Plan Alignment

The NSTC's R&D priorities, facilities, and workforce development efforts are closely aligned with the White House AI Action Plan, ensuring that the U.S. maintains its leadership in AI technologies, which are heavily reliant on advancements in semiconductor technology.

Pillar 1: Accelerating AI Innovation

- ***Investing in AI-Enabled Science and Supporting Next-Generation Manufacturing:*** The NSTC Prototyping and National Advanced Packaging Manufacturing Program (NAPMP) Advanced Packing Piloting Facility (PPF) will lead the world in advancing next-generation manufacturing by providing the first open 300 mm prototyping environment where new manufacturing methods can be leveraged. These facilities will produce the first manufacturing datasets available to researchers, incorporating active feedback in the

[3] Chipping Away. Addressing the Labor Market Gap." Semiconductor Industry Association. July 2023.
[4] Source: Sources: Wallstreet Research, Pitchbook, Factset, 451 Research

prototype line. The Design Enablement Gateway (DEG) will enable IP sharing and the aggregation of design datasets.

- ***Building World-Class Scientific Datasets:*** The NSTC's R&D programs are designed to be powerful data generation engines, maximizing dataset creation to facilitate AI advancements. For instance, the AIDRFIC program requires teams to produce databases of circuit designs, while the TVIP program aims to standardize processes and reduce costs, functioning as a "data generation machine," as described by Andrzej Strojwas (CTO of PDF Solutions). Future programs are structured around the principle of building datasets optimized for AI, ensuring that AI methods are at the forefront of research and development.
- ***Advancing the Science of AI:*** The science of AI and advancement of semiconductor technology are inextricably linked. LLMs and generative AI are dependent on the availability of diverse semiconductor architectures and advances in next generation semiconductor R&D.
- ***Empower American Workers in the Age of AI:*** AI is both changing the skills required of semiconductor talent, as well as creating new tools that are changing the way we prepare people for work. AI has potential to accelerate learning and provide customized support to both students and trainers. The NSTC Workforce Center of Excellence is rapidly scaling training and support to thousands of additional workers to accelerate the development and manufacturing of chips. Natcast will invest in semiconductor industry-related training and educational supports for American workers to help close workforce and skills gaps in the United States for researchers, engineers, and technicians involved in semiconductor design, manufacturing, and production.

Pillar 2: Building American AI Infrastructure

- ***Restoring American Semiconductor Manufacturing:*** Making computer chips, especially AI chips, faster and more power-efficient is a core focus of Natcast's NSTC priorities. The emphasis on advancing semiconductor leadership for the AI era includes prioritizing data centers, which are crucial for AI workloads. The NSTC aims to enhance the security of high-security data centers and edge systems. This involves developing new security solutions, standards, and best practices in collaboration with the National Institute of Standards and Technology (NIST). By focusing on these areas, the NSTC ensures that the infrastructure supporting AI technology is robust, secure, and capable of meeting future demands.
- ***Training a Skilled Workforce for AI Infrastructure:*** The development of AI is dependent on restoring American semiconductor manufacturing and other essential AI infrastructure, which cannot be successful without a skilled and capable workforce underpinning it. The surge in the development and use of AI has fueled increased

demand for diverse chips and has been accompanied by substantial investment in the semiconductor industry. As a result, domestic demand for related talent is projected to dramatically outpace the available supply. Estimates indicate that without proactive action, the available domestic workforce is forecasted to fall short of demand by as many as 67,000 workers[5]. The NSTC Workforce Center of Excellence is fast-tracking workforce initiatives across the United States to bring the U.S. semiconductor and AI chip supply chain onshore and train this essential talent for good-paying jobs in the United States.

Pillar 3: Leading in International AI Diplomacy and Security

- ***Align Protection Measures Globally***: Protecting U.S. leading-edge chips from reaching adversaries like China is a priority for maintaining America's competitive edge in AI technology. The NSTC has established stringent evaluation and security measures for its research projects from the outset. These measures can be shared and aligned with international research partners.
- ***Plug Loopholes in Existing Semiconductor Manufacturing Export Controls:*** Beyond enforcing strict export controls, the NSTC emphasizes the importance of provenance and traceability for tracking the distribution and usage of chips. The exploration of DRM-like technologies will play a crucial role in protecting intellectual property, licensing usage, and preventing tampering or unauthorized use. The Hardware Security & Provenance theme ensures that U.S. advancements in semiconductor technology are safeguarded against misuse.

The NSTC's alignment with the White House AI Action Plan underscores its commitment to maintaining and expanding U.S. leadership in AI technologies. By accelerating AI innovation, building a robust AI infrastructure, and leading international diplomacy efforts, the NSTC ensures that the U.S. remains at the forefront of AI advancements, driving progress and securing its technological future.

[5] Chipping Away. Addressing the Labor Market Gap." Semiconductor Industry Association. July 2023.

3. Grand Challenge Opportunities

The ability to harness the unique facilities and deep technical expertise of Natcast staff and Member companies positions the NSTC for undertaking high-risk, high-reward research and development on an accelerated timeline.

Grand Challenge 1: Improve performance and energy efficiency for AI data centers by 1000x by 2035

The primary objective is to enhance performance and energy efficiency for AI data centers by 1000x by 2035. Six specific research opportunities related to this objective address nearly every aspect of semiconductor technologies used within the data center, with the goal of maximizing AI performance and minimizing energy consumption. The areas of focus include the entire semiconductor compute stack: compute logic, all layers of the memory hierarchy, on-die interconnect, 3DIC advanced packaging, photonic interconnects, power delivery, and thermal and cooling solutions.

- **Novel Device Architectures to Improve Device Performance, Power, and Area (PPA)**
  - As the advantages derived from traditional Moore's Law scaling have waned, future enhancements will be achieved through innovative materials and architectures. This research opportunity encompasses transistors (including CFET and beyond), interconnects, and memory technologies.
- **Ultra-fine Pitch 3-dimensional integrated circuit (3DIC) Application Exploration and Enablement**
  - 3DIC technologies with ultra-fine pitches of less than 700 nm will facilitate innovative chiplet partitioning strategies, advance design methodologies, enhance thermal extraction systems, and integrate power delivery networks.
- **Energy Efficient Power Devices and Package Level Power Delivery**
  - Enhancements in power delivery and conversion efficiency encompass the use of wide band gap materials, innovative power device architectures, as well as on-die and in-package integration techniques.
- **Energy-Efficient High-Bandwidth Data Center Interconnect**
  - AI data center connectivity is expected to improve with ultra-dense, high-speed, and energy-efficient electro-photonic interconnects that facilitate chip-to-chip and package-to-package data transfer. Key research areas include developments in light sources, materials, device architectures, and packaging techniques.
- **Transformative AI System Architectures**
  - Innovative architectural strategies have the potential to significantly enhance system-level performance. Research will encompass novel computing paradigms and architectures, including advanced accelerators and memory sub-systems.

- **Cross-Stack System Innovations**
    - A key challenge in hardware engineering is predicting how changes to components affect the entire system. This research focuses on evaluating performance, power, thermal, and cost trade-offs, and identifying technology developments that maximize return on investment at the system level.

Grand Challenge 2: Establish Leadership in American-Made AI Chips

At present, no AI chips are entirely manufactured in the United States. Consequently, Grand Challenge #2 is to re-establish U.S. semiconductor manufacturing leadership, thereby securing U.S. dominance in the complete AI stack. A crucial factor for regaining manufacturing leadership is EUV (extreme ultraviolet) photolithography, which represents the most advanced and costly segment of producing cutting-edge semiconductor chips and is currently monopolized by a single non-U.S. company. There are also other R&D areas where global competitors are investing and seeking to take the lead in chip manufacturing. By focusing on this promising R&D portfolio, the United States can achieve leap-ahead technology developments domestically.

Research focus areas include:

- **Enhance EUV Capabilities**
    - It is anticipated that future process nodes will necessitate resolution that exceeds the capabilities of current tools from a single exposure. Therefore, research into Hyper-NA EUV and wavelengths beyond EUV will be essential to support single exposure pitches at 16 nm and below.
- **Mature EUV Augmentation and Alternatives**
    - With the increasing cost of EUV, patterning approaches that provide similar performance at a lower cost will be considered. This includes enhancing EUV with directed self-assembly processes and advancing alternative methods such as nanoimprint lithography.
- **Improve Design Efficiency**
    - Artificial Intelligence and Machine Learning techniques for digital, RF, and analog/mixed signal design will be employed to mitigate the rising design costs and to democratize innovation by utilizing shared training datasets.
- **Scale 3D Intelligent Failure Analysis**
    - Complex 3D architectures, including backside power delivery, Gate-All-Around transistors, and 3DIC packaging, present significant challenges due to buried defects being deeply encapsulated within material stacks. Research efforts are focusing on the development of advanced diagnostic tools, intelligent automation, and design-to-silicon traceability to expedite root cause identification and improve fault visibility across heterogeneous systems.

Grand Challenge 3: Double Semiconductor Investment Exits in the U.S. AI Stack, Catalyze $5 billion in new VC Investment, and Launch a National AI Data Center Validation Lab

While AI startups are gaining popularity in the current economic climate, the semiconductor and AI hardware ecosystem is often misunderstood or overlooked by traditional venture capital funds. To date, there has been a ~90% dropoff in the number of successful exits for US semiconductor industry start-ups via IPO on U.S. stock exchanges since 2007[6].

In addition, there has been a significant decline in the rate of private sector funding for semiconductor startups. In 2008, 4.3% of all VC dollars went into semiconductors ($1.6B out of $37.1B) and it has trended down since then. Less than 1.5% of all VC dollars have gone into semiconductors annually since 2015, including only 1.2% in 2022 ($2.8B out of $240.9B invested across all sectors)[7]. The NSTC Semiconductor Innovation Fund (SIF) has the potential to catalyze private sector capital and drive more successful exits for U.S. semiconductor startups by deploying capital effectively.

- The SIF aims to target investments in promising early-stage companies that develop critical AI-related semiconductor technologies. This will provide the necessary capital to achieve crucial milestones such as commercial prototype development, pilot production, and securing initial customers. These investments will focus on targeted areas of the full AI stack, ensuring that future technology driving the "AI Factories" of the future is based in the United States.
- To unlock the next wave of AI infrastructure innovation and catalyze investment in U.S.-based AI hardware, the NSTC can establish a National AI Data Center Validation Lab. This facility will enable startups to validate their technologies at data center scale – an essential step before adoption by hyperscalers – closing a critical gap in the commercialization process. In partnership with industry leaders, this lab will complement SIF's catalytic capital by providing real-world testing environments, accelerating time to market, and further crowding in private investment across the AI stack.
- Utilizing unique "crowd-in" approaches for premium investments in the semiconductor and AI stack ecosystem, the SIF encourages co-investment from private capital to participate in earlier rounds of venture capital funding, bridging the widening later stage private capital funding gap for promising startups focused on the AI technology stack. These "crowd-in" strategies can raise nationwide VC investment by a few percentage

[6] IT Semiconductor Industry Analysis: NSTC Investment Fund Final Report - November 2023
[7] Wall Street Data, Pitchbook.

points, but as rounds progress, can result in multi-billion dollar increases. Such increases in investment will revitalize the American Dream for AI semiconductor entrepreneurs.

- Access to capital is a major valley of death for semiconductor innovation. By identifying the best potential investments from across the NSTC ecosystem – that are often missed or under-funded by traditional venture capital coverage – the SIF can uniquely increase the rate of successful exits among U.S. semiconductor startups. These successful exits will return the invested capital to the NSTC and benefit the American taxpayer, encourage more long term private sector capital into a flourishing investment sector, and continue to expand the U.S. semiconductor innovation ecosystem.

4. NSTC Progress for 2024-2025

The establishment of Natcast came after an extensive review of whitepapers and proposals from various industry consortia which included participation from various Chief Technology Officers, Senior Vice Presidents of Research, and other leaders from across the semiconductor supply chain. These consortia included the Department of Commerce's Industrial Advisory Committee, the President's Council of Advisors on Science and Technology, the IBM-led ASIC Coalition, and the MITRE-led Semiconductor Alliance. In addition, the Commerce Department also evaluated several models such FFRDC's and other public-private partnership modalities and found key weaknesses that would slow down the speed and progress of the newly envisioned entity.

It became evident that only a new, purpose-built organization, Natcast, could promise the technology and industry neutrality required to engage with all the key activities tasked to the NSTC – such as establishing critical R&D services that are currently unavailable in the United States but exist elsewhere, addressing the workforce shortage, and jump-starting the startup-to-venture capital pipeline for semiconductors in the United States..

Congress mandated the creation of a public-private consortium and specifically authorized the use of its Other Transaction Authority (OTA) contract, with the intention of providing flexibility to the Commerce Department in setting up this new public-private partnership. Ultimately, the creation of Natcast, the non-profit entity designed to operate the NSTC, followed existing precedents around the use of OTAs to expedite expanding the U.S. industrial base. This approach included a call for a team to form in partnership with the Department of Commerce (DOC), a method also used in the founding of the Aerospace Corporation in 1960, ICANN in 1998, NTCC in 1990, and In-q-tel in 1999.

Chips Research and Development Office (CRDO) and Natcast issued several RFI's and engaged with industry, academia and governmental stakeholders across the semiconductor ecosystem,

resulting in a total of 700+ engagements and releasing of the NSTC Strategic Plan FY25-27[8] that centered around the following goals:

1. Extending U.S. semiconductor leadership
2. Reduce time and cost to prototype in the U.S.
3. Build a robust U.S. workforce ecosystem

From May 2024 through January 2025, leveraging the NSTC Strategic Plan as well as 80+ responses to an RFI focused on facility capabilities[9], the Facilities Assessment and Siting Plan commenced with assistance of a highly experienced strategy consulting firm and CRDO. The Facilities team evaluated 386 Metropolitan Statistical Areas for semiconductor talent, companies, educational institutions, and capabilities. All 56 U.S. States and Territories received 21 targeted questions regarding their semiconductor ecosystem. This resulted in 30+ sites visited, 150 detailed questions on individual sites, and 30+ due diligence interviews prior to the three announced site selections[10].

In May of 2025, the NSTC Technology Advisory Board (TAB) was announced, a significant milestone for the NSTC. With a breadth of experience across the semiconductor supply chain, TAB members represent a significant collective brain trust, ensuring that the goals of the NSTC are informed by the leading minds of the semiconductor industry. The TAB ensures technical relevance and risk-taking, neutrality, and industry buy-in. Further, the establishment of the TAB drives down risk for taxpayer funded NSTC research by encouraging industry adoption of NSTC-developed technologies, increasing the return on investment for NSTC funded R&D.

In the spring and summer of 2025, the NSTC R&D division collaborated with the TAB to develop the priorities. They have proposed a comprehensive R&D grant program to bridge across the numerous and varied "valleys of death" in U.S. semiconductor R&D. This includes grant opportunities to support high-risk, high-reward technologies and innovative semiconductor advancements. The proposed in-house R&D capability will allow NSTC to work with industry and academia to evaluate promising and technically sound projects.

Additionally, the NSTC Workforce Center of Excellence (WCoE) is working to develop the skilled workforce required to advance the U.S. semiconductor industry. The center launched in the Fall of 2024, and established the NSTC Workforce Awards Program on July 1, 2025, creating a nationwide fund to support projects that address a critical workforce need in the U.S. semiconductor industry and close key skills and labor market gaps. The program is expected to serve tens of thousands of American workers over the course of the next decade, preparing

[8] "NSTC Strategic Plan FY25-27." Released Oct. 2024. Note: the NSTC Strategic Plan is currently undergoing its annual update, with anticipated release date of Oct. 2025.
[9] "Facilities Model Fact Sheet". July 2024.
[10] "CHIPS for America and Natcast Site Selection Criteria." July 2024.

them for careers in roles as researchers, engineers, and technicians in semiconductor design, manufacturing, and production.

The Workforce Center of Excellence's work is guided by input from its Workforce Advisory Board (WFAB), which was established in January of 2025 and consists of senior leadership from America's leading semiconductor companies and academic institutions. The WFAB offers strategic advice to the WCoE on how it can address the challenges faced by stakeholders in semiconductor workforce development, contributing expertise and insights to the WCoE's work and ensuring it adapts to the ever-evolving demands of the industry.

Finally, the Semiconductor Innovation Fund aims to provide the necessary funding and resources to startups and small businesses in the semiconductor field, fostering innovation and ensuring a steady pipeline of new technologies. Currently, there is a lack of private sector funding for semiconductor startups, and therefore, the fund will catalyze early venture financing rounds by providing capital that is less dilutive to both companies and early investors. In the long term, the fund aims to increase the number of U.S. successes in the semiconductor and AI ecosystem stack, bringing more venture capital investment back to the sector. Ultimately, the seed capital for the SIF will be returned to the taxpayer.

5. NSTC Facilities

The selection of NSTC facilities ensures there will shortly be a whole-of-nation capability offering a national "full flow" of semiconductor manufacturing and R&D. This is a radical – and critical – new development for the United States.

Prior to the establishment of Natcast and the NSTC, doing this type of semiconductor R&D required waiting months to years in either Taiwan or Belgium and/or paying millions of dollars in fees. This monopoly of semiconductor R&D capabilities overseas has been a significant factor in diminishing the ability for next generation semiconductor manufacturing and design technologies from prototyping in the U.S., pursuing R&D patent filings, developing talent in the U.S., and ultimately, going public in U.S. markets.

The NSTC facilities include the following:

- **Extreme Ultraviolet (EUV) Lithography Accelerator in Albany, New York.** The EUV Accelerator provides NSTC Members access to an established EUV research facility, including access to a leading edge 2 nm process technology, including the running of wafers[11], that Members can use for research and development purposes. Members

[11] Wafer runs at the EUV Accelerator can include full flows that are aligned with the production of advanced logic chips. This is the same the commercial flow used by Rapidus in Japan but does not include memory chip full flow or AI chip full flow.

currently have access to a standard resolution and will soon have access to a high resolution high-Numerical Aperture EUV lithography toolset in 2026-2027.

Given the prohibitively high costs for both the EUV lithography tools as well as for leading edge process development, access to EUV-based processes and tools within the semiconductor ecosystem has been severely limited. The NSTC EUV Accelerator is solving this challenge with cost effective access to these capabilities, and through collaboration with NSTC Members, is accelerating semiconductor technology leadership in the United States. This initiative has outsize impact on developing the U.S.-Japanese allied ecosystem, and capturing leadership in next-generation semiconductor materials, designs, and chip architectures.

- **Design Collaboration Facility (DCF) in Sunnyvale, California.** Located in the heart of Silicon Valley, the DCF convenes and facilitates co-creation opportunities with leading NSTC Members. It also includes "dry labs" with chip bring-up services that will enable startups, researchers, and industry leaders to co-develop and test new designs, materials, devices, and packaging solutions using state-of-the-art equipment. The dry lab is designed to support end-to-end pre-silicon and post-silicon system level testing of chips across all verticals. This includes full stack testing for AI designs, IPs, and infrastructure.
- **Design Enablement Gateway (DEG) and Silicon Aggregation (SiAgg) services in Sunnyvale, California.** Design Enablement Gateway (DEG) is a platform offering tools, cloud infrastructure, and an IP marketplace to speed up the journey from concept to prototype. Given the extensive semiconductor expertise needed – from architecture to manufacturing – DEG also provides staffing, methodologies, and technical consulting for NSTC members. This encompasses digital, analog, and mixed signal designs across areas like data center AI, edge AI, HPC, networking, storage, and memory. Silicon Aggregation negotiates with foundries to reduce costs and development time. Ultimately, DEG and SiAgg aim to drive onshore U.S.-based semiconductor prototyping for EUV Accelerator, the PPF, and at private sector and academic NSTC members.
- **NSTC Prototyping and National Advanced Packaging Manufacturing Program (NAPMP) Advanced Packaging Piloting Facility (PPF) in Tempe, Arizona.** The PPF is a critical NSTC/NAPMP facility that will provide the U.S. R&D ecosystem access to a comprehensive suite of advanced technologies from silicon start through advanced packaging, and stable CMOS and Advanced Packaging technology flows to evaluate their innovations. Full prototyping for CMOS and Advanced Packaging will be available within the same facility, significantly reducing the time and cost for R&D innovation proof of concept and prototyping, a capability currently unavailable in the U.S. or other parts of the world. It is important to note that the PPF process will be further refined and defined based on the proposed NSTC R&D priorities.

  In 2025, the PPF site selection team identified the location for this facility at the center of the Arizona State University (ASU) Research Park in Tempe, Arizona. The ecosystem in

this region is exceptionally strong and continuously growing, with substantial presence in Advanced CMOS manufacturing as well as being one of the few places in the U.S. with an Advanced Packaging Manufacturing Ecosystem. An architectural and engineering firm has been engaged, and project programming/pre-design is actively underway with the objective of breaking ground by the end of 2025.

Brokering and Unlocking Capabilities

As the largest non-private buyer and broker of semiconductor R&D tools, equipment, and software, the NSTC has undertaken a "Costco" model for membership for all parts of the semiconductor supply chain[12]. The EUV Accelerator DEG, and SiAgg offer highly cost-effective wafer runs, design resources, including EDA tool licenses, and other design collateral, to enhance research relevance and impact for universities, researchers, startups, and small and mid-size business seeking to expand their semiconductor R&D portfolios.

For example, the Test Vehicle Innovation Program (TVIP) provides specialized and advanced test structures and wafers from semiconductor foundries to NSTC Members engaged in research. This aims to standardize dataset creation relevant to AI-enabled semiconductor R&D and enhance industrial relevance. One TVIP project can lower the cost of testing a memory device on an industrially relevant platform from $18M in design and mask sets down to as low as $100K, with each foundry wafer costing around $3,400. The NSTC will distribute this type of prototyping capability to university nano-centers across the nation, integrating directly with the National Nanotechnology Infrastructure Network.

Natcast is also address the current limitations faced by U.S. semiconductor researchers by brokering near-term access to other existing facilities and specialized capabilities. By partnering to "unlock" joint capabilities with U.S. Department of Energy National Labs, universities like Purdue, ASU, MIT and Georgia Tech, and the private sector, the NSTC can facilitate both cost-recovery and widespread crowd-in investments in semiconductor R&D in the United States[13].

Further, the NSTC's facility strategy, especially combining the EUV Accelerator and PPF, provides several strategic benefits. These include:

- **Streamlining Semiconductor R&D Red Tape:** Existing R&D facilities within the continental United States often operate with limited autonomy and face known accessibility issues, particularly related to intellectual property concerns. In contrast, NSTC facilities offer independent priorities-setting and greater flexibility.

[12] The DEG See Natcast submission to DOC. "DEG Strategy Document", "SiAgg Strategy Document". 06/30/25.
[13] "The Returns to Public R&D". Fieldhouse and Merkels. Federal Reserve Bank of Dallas, Mays School of Business at Texas A&M. NBER Entrepreneurship and Innovation Policy Conference, 2025.

- **Radically Scaling U.S. Semiconductor R&D Capacity:** Many existing facilities are near their R&D capacity and would require significant capital expenditure for expansion, whereas for example, the PPF's greenfield opportunity allows for scalable capacity. These facilities will also support U.S. workforce development efforts by providing opportunities for collaborative, hands-on training and research.
- **High-Risk, High-Reward, Leap-Ahead Semiconductor R&D:** NSTC facilities are also better positioned to explore and integrate new capabilities, providing full process data for federated models.
- **Flexibility for Emerging Concerns:** Furthermore, NSTC facilities include a 30k square feet placeholder for private cleanroom lease, addressing the limited sublease options available in many current facilities.

6. Conclusion

The NSTC's uniquely flexible public-private structure, fast go-to-market actions, and unprecedented nationwide facilities and R&D infrastructure present a rare opportunity to shape the future of U.S. semiconductor and AI leadership for a more prosperous, competitive, and secure leadership position for the United States.

Appendix

Natcast and Gold Standard Science Executive Order

In May and June of 2025, after the release of the Strategic Plan, Natcast confirmed that the NSTC's approach to R&D is aligned with the principles of "Gold Standard Science,"[14] generating research that is reproducible, transparent, and communicative of errors and uncertainties. NSTC research will be collaborative and interdisciplinary, skeptical of its findings and assumptions, structured for falsifiability of hypotheses, subject to unbiased peer review, and accepting of negative results as positive outcomes, all while avoiding conflicts of interest. These principles will be embedded in the research processes to enhance the integrity and reliability of scientific findings.

Natcast Requests for Information 2024-2025

R&D

- Interconnect Materials and Integrated Processes for Power-Performance-Area (PPA) Improvement in Compute Applications (July 2025)
- Co-packaged Optical Engine Development for AI Infrastructure Scale-up (July 2025)
- Low-Dimensional Materials for Power-Performance-Area Optimization in Logic Applications Beyond CFET (May 2025)

Facilities

- R&D Prototyping Facilities and Capabilities: Use Cases and Market Demand (March 2024)

NSTC Strategic Plan FY25-27

- Link here
  Note: an annual revision to the NSTC Strategic Plan has been submitted to DOC for review, anticipated release is Oct. 2025.

How the NSTC Increases the ROI of Semiconductor Research

NSTC research programs will address these grand challenges using an approach that is differentiated and will maximize overall return on investment. NSTC's unique approach to research includes a combination of funding, access to state-of-the-art facilities, standardized test and reporting infrastructure, and methodologies to support reproducibility and benchmarking.

[14] "Restoring Gold Standard Science." Executive Order. May 23, 2025.

	Challenge	Action	Expected Result
1.	**Funding:** Lack of funding for research that targets the lab-to-fab gap, i.e., after pre-competitive research traditionally funded by government yet before there is a clear path to commercialization	Invest almost $4 billion in competitively awarded funding that is in alignment with a **Member-driven** priorities and leveraged with industry investment	Accelerated research that translates promising experiments to commercial viability; breakthrough innovations that drive U.S. leadership in semiconductors
2.	**Access:** Limited or no access to advanced manufacturing tools, process flows, and design resources making it difficult and costly to scale and repeat lab successes	Harness the American entrepreneurial engine by employing close to $2 billion to **increase access** to commercial-grade R&D facilities, including advanced fabrication and design	Increased research relevance and reproducibility that advances the commercial readiness levels of key technologies and speeds breakthroughs that can scale
3.	**Consistency:** Lack of consistency in test structures, test methodologies, and reporting infrastructure that drives the cost of test chip experiments to the millions of dollars	Facilitate common sets of **standardized** test structures and methodologies that reduce one-off costs (e.g., non-recurring engineering) and increase the availability of complex templates (e.g., photomasks) in research manufacturing	Consistent, high quality, and low-cost testing structures and methods that are available broadly to NSTC members to lower the time and cost to prototype
4.	**Transparency:** Less-than-comprehensive results reported through conferences and publications, with representation weighted to successful experiments and established institutions	Create platforms for aggregating and sharing results, including negative and neutral results that often go unreported, to support **benchmarking and reproducibility**	More comprehensive understanding of research outcomes to reduce research inefficiencies and accelerate the pace of U.S. innovation