Natcast

Natcast Assets

Enabling assets providing national value and supporting the continued mission of the NSTC

September 2025

Executive Summary

Natcast has invested 18+ months in building and optimizing multiple high-impact national assets to accelerate U.S. semiconductor R&D, develop a skilled workforce, and strengthen our economic and national security.

By engaging, connecting, and understanding the U.S. semiconductor ecosystem through…

- 1,000+ ecosystem inputs; 6+ deep-dive reports
- 200 Members; 1,500+ prospects in CRM
- 30+ collaboration events; 4,700+ participants
- 60+ startup pipeline; 100+ syndicate investors
- 39 esteemed semiconductor research and workforce leaders on NSTC Advisory Boards
- Deep relationships throughout the ecosystem
- Thorough understanding of existing capabilities, demand, and gaps throughout the value chain

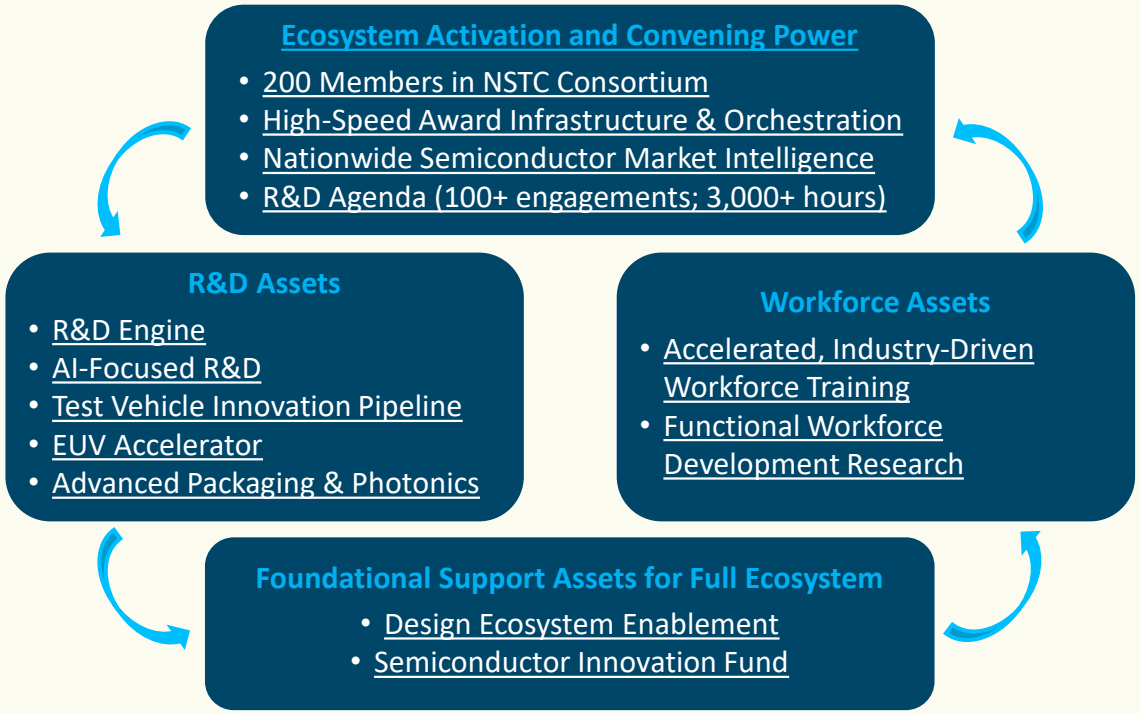
Natcast has developed valuable national assets which are…

- Focused on the R&D “valley of death” (TRL/MRL 3-7) to advance promising innovations from lab-to-fab
- Creating infrastructure to reduce time from concept to prototype by 30%; “0 to 1” capabilities for 100+
- Driving toward an industry-created Research Agenda
- Developing a skilled domestic semiconductor workforce for the industries of today and tomorrow
- Moving at the pace of industry (2x speed of gov’t)
- Scalable and forward-looking to account for future needs in this rapidly evolving industry

Assets Overview

Value to the Nation: People, processes, relationships, and technologies performing 2x more efficiently than USG programs

Value Overview: Leverage deep understanding of ecosystem to develop assets which address need, accelerate innovation, and build workforce:



In-House Operational Excellence Assets

- 2x faster than pace of government
- Overhead forecasted at 10% of CHIPS funding over 10 years
- 119 deliverables & milestones submitted to DOC since April 2024
- 59 policies and procedures established (incl. 13 security-related)
- $1.5M of cost savings across 100 contracts totaling $20M
- $30M+ in FY24-FY26 consulting cost avoidance by thru in-house teams

Comparables

Natcast Advantage	Natcast Example	Traditional Government Example
1.5–2x times faster advanced R&D proposal evaluation	AIDRFIC Awards - 8.5 months	Federal Agency - 14 months
2–3x times faster workforce competitions	Workforce Partner Alliance Program (WFPA) – 86 days	DoL ETA's Strengthening Community Colleges Training Grants – 238 days
50-75% less overhead than academic + international peers	Forecasted Overhead <10% of Expenses	Average R&D Overhead Costs: USG (15-30%), University (30-40%), Non-Profit (25-40%), IMEC/Leti/ITRI (20-45%)

Expertise

Team	Team Size	Avg Years Experience	Advanced Degree Holders	Areas of Expertise
Research	21	20	15	EE, Chem E, Materials Science, Photonics
Workforce	16	16	11	Labor Market Analysis, Grant Making, Program Evaluation, Sector Partnerships, Education and Training Systems, Education Reform, Data Analysis
Investment	5	26	4	Electrical and Chemical Eng., Materials Science, Economics, Finance
Design Ecosystem Enablement	11	26	9	EDA, Tape-outs, Labs, System-level Design/Validation
EUV	6	22	4	EUV, Photonics, Process Integrations, Packaging
Membership + Ecosystem	16	17	2	Process and Packaging Technology, Materials Science and Engineering, AI/ML Deployment
Support Functions	35	17	26	Law, Finance, HR, Accounting, Econ, Math

Note: Click the underlined hyperlinks above to go directly to their respective detailed Asset description.

Natcast

NSTC Consortium Membership – 200 and Growing

Enables real-time insights from across the U.S. semiconductor ecosystem. Identifies industry needs, connects ecosystem to existing infrastructure and capabilities, and drives collaboration.

Driving Speed to Innovation → **Accelerating Ecosystem Development** → **Solving the Workforce Gap**

Natcast

Ecosystem Activation & Convening Power

Asset type:
- ❑ Driving Speed to Innovation
- ☑ Accelerating Ecosystem Development
- ❑ Solving the Workforce Gap

Value to the Nation: Harnessing U.S. semiconductor leadership through consortium development; built on deep industry insight, enduring relationships, and a purpose-built framework for accelerated innovation

Value Overview

Convening force of the U.S. semiconductor R&D ecosystem, serving as the national hub for collaboration, insight, and coordinated execution. Through the NSTC, Natcast bridges academia, industry, national labs, startups, and government, ensuring that research priorities are aligned with U.S. policy objectives, including the AI Action Plan and CHIPS Act mandates. This covers the governance, strategic planning, and outreach mechanisms that allow Natcast to mobilize the semiconductor ecosystem rapidly, respond to emerging technology priorities, and embed U.S. leadership in AI-relevant semiconductor development.

Components

Component	Description
Agile Agenda-Setting	Dynamic, member-informed GTM framework, designed to be adaptable and fast-moving, while aligning with the needs of the ecosystem and U.S. Engages stakeholders across every layer of the integrated design stack. Insights serve as the foundation for high-impact programs designated to engage prospective members and enable unprecedented cross-sector collaboration.
Strategic Relationship Management	Rooted in decades of trusted relationships across the semiconductor industry, leverages multiple connection points (advisory board seats, convenings, focus groups, Communities of Action, formal Requests For Information, workshops, 1:1 touchpoints) to prioritize mutual discovery and ensure continuous value delivery.
Actionable Insights	Critical insights into pain points and high-priority opportunities identified through targeted discussions. Navigator service launched to build extensive knowledge base of Member capabilities and pipeline to National Lab resources, unlocking streamlined access to existing R&D infrastructure.
Revenue Management	Revenue forecasting system from NSTC Facilities, including process for identifying and tracking member usage. Built $9.6M pipeline to support financial objectives for EUV Accelerator through deep discovery and collaboration. Developed pricing model that balances industry 'willingness to pay' and Natcast financial obligations.
Foundational CRM	Comprehensive infrastructure to track segmentation, engagement, and targeted campaigns across 200 members and 1,500+ prospects.

Investment to Date

Investment	Details
2,580+ work hours and $4.5M+ to aggregate data and build knowledge base	• Expert consultation to strategically collect data, integrating critical insights to build services that address industry needs. • Dynamics CRM deployed containing data that feeds high-impact programs.
3,292+ work hours and $1.5M+ in custom development to deploy scalable infrastructure	• Custom system in-development to track 360° orchestration of activity. • Collaborative discovery in-process to build personalized journeys, containing marketing automation and an external-facing member portal. Full implementation ~40% complete.

Relevant In-House Expertise

Team Size	Avg Years Relevant Experience	Advanced Degree Holders	Team-wide Accomplishments
17	**19**	**2**	• Industry Experience: Analog Devices, GlobalFoundries, IBM, Micron. • Acquired 200 members in 11 months, including 17 companies listed on the 2025 Fortune U.S. 500 or Global 500. • Deployed CRM in 20 days; Orchestrated 15 high-value Navigator connections in 6 weeks; Hosted 32 events; Produced 22 press releases.

Subdivision Name	Areas of Expertise
Business Development & Membership Acquisition	International Partnerships, Relationship Management, Forecasting; Prospecting, Multithreading, Negotiation, Deal Closure, Value-Based Selling.
Membership Engagement	Market Research, Competitive Analysis, CRM Lifecycle Management, Community Engagement & Multi-Channel Strategy, Audience Segmentation.
Marketing & Communications	Storytelling, Brand Strategy, Media Relations, Executive Communications, Digital Strategy, Marketing Automation, Events Management.

High-Speed Competitive Award Infrastructure

Asset type:
- ☑ Driving Speed to Innovation
- ☑ Accelerating Ecosystem Development
- ☑ Solving the Workforce Gap

Value to the Nation: addressing critical industry needs as they arise in less than half the time it takes government, driving U.S. semiconductor innovation at maximum efficiency

Value Overview

Designed to execute large-scale competitive workforce and semiconductor R&D investments swiftly and flexibly. Utilizing OTA mechanisms and custom operational playbooks to launch multi-domain research or workforce competitions within weeks. Rapid deployments address global competitive pressures in the AI Action Plan, such as AI chip design, advanced manufacturing, workforce and semiconductor security.

Components

Component	Description
Competition & Award Playbooks	Step-by-step framework for running high-impact funding competitions with speed, precision, and transparency. Covers pre-announcement planning, RFI/CFP drafting, evaluation criteria, award selection, post-award management and performance monitoring. Includes RACI charts, SIPOC diagrams, rubrics, reviewer trainings and standardized templates.
Program Design Toolkit	A repeatable framework for creating multi-domain R&D and workforce programs. Includes domain-specific operational playbooks, rapid-deployment checklists and automated workflows that dramatically reduce launch timelines compared to traditional federal programs. Adaptable to address respond to emerging national priorities and scale to accommodate projects of varying complexities.
Flexible OTA Funding Mechanism	Accelerates the pace of innovation by reducing administrative bottlenecks and enabling adaptive award structures. Allows for faster contracting, tailored terms, and streamlined compliance, ensuring resources are delivered to research teams when needed most.
Research Security & IP Protection	Program compliant to NSPM-33, certified by NIST. Safeguards sensitive data and intellectual property in multi-party research environments.

Investment to Date

Investment	Details
4,783+ work hours in process design, award system configuration and implementation	• 50+ flexible, re-deployable operational/process assets. • 10+ automated tools to streamline execution. • Tested and refined over 4 large R&D award programs and 2 workforce award programs launched to date.
2,625+ work hours in financial and legal contractual structure and vehicle design	• Legal templates for NDAs, IP agreements, and data-sharing arrangements. • Strategies for equitable and collaborative IP management. • Cost-effective delivery vehicle design.
2,910+ work hours in Research Security and Operations	• Scalable protocols for handling controlled and export-restricted information though technology control plans (TCPs). • Cleared and actively monitoring 58 organizations and 342 individuals across active research programs. Scalable to support 300+ employees, 1,000+ researchers, 2,500+ construction workers.

Relevant In-House Expertise

Team Size	Avg Years Relevant Experience	Advanced Degree Holders	Team-wide Accomplishments
22	15	12	Deployed rapid, flexible award infrastructure in weeks; safeguards IP + research security, addresses urgent national technology priorities.

Subdivision Name	Areas of Expertise
Awards Program Management	Program Evaluation, Performance Monitoring, Competitive Funding Administration, Portfolio and Compliance Oversight, Merit Reviewer Training, R&D and Workforce Strategy, Economic Development, Volunteer Coordination, CRM Development, Fundraising.
Research Security	Counterintelligence and Foreign Affairs Expertise with DoD, DOE, and U.S. Department of State.
Finance	Federal Funding Compliance, Monitoring, Audits, Invoicing.
Legal	IP Management, Patent Portfolio Oversight, Foreign Policy.

Nationwide Semiconductor Market Intelligence

Asset type:
- ☑ Driving Speed to Innovation
- ☑ Accelerating Ecosystem Development
- ☑ Solving the Workforce Gap

Value to the Nation: Market intelligence team with the only fully comprehensive understanding of the U.S. R&D and workforce ecosystem—capabilities, demand, investments, and gaps across the entire value chain

Value Overview

Comprehensive understanding of the current U.S. semiconductor ecosystem, ranging from startups to the biggest industry players, to educational institutions, and government organizations. Deep institutional knowledge developed from synthesizing hundreds of conversations and written insights from throughout the ecosystem.

Components

Component	Description
U.S. Semiconductor R&D Facility Supply & Demand Intelligence	Synthesis of 80+ responses to the 2024 RFI, "Semiconductor R&D Prototyping Facilities and Capabilities: Use Cases and Market Demand." Categorizes responses across 98 different demand factors ranging from desired tech nodes to process flows to substrates. Compiles current supply-side R&D capabilities in use.
Insight into Ecosystem at MSA (Metropolitan Statistical Area)	Analysis of current nationwide semiconductor capabilities, talent, industry presence, research labs, R1 universities, investors, and startups across each MSA within U.S. Over 30 due diligence conversations with semiconductor stakeholders and a deep-dive analysis of single site capabilities across various regions.
Analysis of Semiconductor Startup and VC Landscape	50+ conversations with semiconductor startups and VCs and a heavy quantitative analysis of 8,000+ semiconductor deals from 2008-2023 captured by Pitchbook. Insight into deal flow, including average round sizes by semiconductor technology over time, the major investors and acquirers, and typical exits.
R&D Ecosystem Gaps Analysis	Synthesis of major gaps in the U.S. R&D ecosystem as captured in over 50 conversations with semiconductor stakeholders. Includes a supply chain analysis and recommended solutions.
NSTC Financial Model and Operational Framework	Analysis of operational requirements to solve ecosystem gaps and a bottom-up and top-down financial analysis of each operational requirement. Financial model includes 1,000+ inputs, 30+ scenarios, and an initial Total Addressable Market.
Innovation Ideas from the Ecosystem	720+ responses to RFI and proposals for research opportunities to advance semiconductor technologies and enhance U.S. leadership.
National Workforce Supply Analysis	Analysis of U.S. academic programs identified by cross-mapping industry role requirements against comprehensive national educational datasets.

Investment to Date

Investment	Details
50,000+ work hours and $7.5M in developing reporting	• 150+ conversations with leaders across the semiconductor ecosystem. • Deep-dive understanding of demand for prototyping capabilities. • Multiple analyses on workforce, investors, and startup landscape.
2,500+ total hours reviewing 720+ total RFI responses	• In-depth understanding of multiple ecosystem innovation pathways and technical solutions.
10,000+ work hours and $2.1M in developing configurable workforce landscape data tools	• Initial strategic analyses for the Workforce landscape. • Sets baseline snapshot of the U.S. workforce development landscape in 2022, leveraging data from 149 industry-aligned programs. • Data compiled at credential, program, location, and institution levels.

Relevant In-House Expertise

Team Size	Avg Years Relevant Experience	Advanced Degree Holders	Team-wide Accomplishments
11	**20+**	**6**	Developed 6+ reports (500+ pages), 2 dashboards, and a long-term financial model

Subdivision Name	Areas of Expertise
R&D Market Intelligence	Stakeholder Engagement, CRM Management, Surveying, Quantitative and Qualitative Analysis, Synthesis, Data Visualization.
Workforce Market Intelligence	Longitudinal Research, Causal Inference, Big Data, Economics, Scenario Modeling, Micro and Macro Economics, Data Visualization, Program Evaluation, Advanced Statistical Research, Multiple Regression Analysis, Cluster Analysis, Focus Groups, Thematic Analysis, Skill-Level Analysis, Career Pathing, Labor Trend Analysis, Domestic Workforce Policy, Federal Datasets, State Workforce Development Systems, Data Visualization Design.

Natcast

R&D Engine: Expertise, Agenda, and Programs

Asset type:
- ☑ Driving Speed to Innovation
- ☑ Accelerating Ecosystem Development
- ☐ Solving the Workforce Gap

Value to the Nation: Transforming U.S. research into fab-ready technologies that power innovation, jobs, and national security

Value Overview

Differentiated approach of research enablement, aggregation, and orchestration driving an end-to-end pipeline for turning breakthrough semiconductor ideas into commercial reality. Spanning the full lifecycle from concept and competitive selection to fabrication, testing, dataset generation, and market transition, it unites world-class facilities, tools, datasets, and talent into a single national R&D capability. By bridging the lab-to-fab gap, enabling secure data sharing, standardizing test and reporting methods, and providing flexible OTA-enabled funding, the Research Engine accelerates innovation, advances U.S. leadership in AI and semiconductor technologies, and ensures that every project delivers maximum impact.

Components

Component	Description
Integrated Lab-to-Fab Pipeline	Covers full lifecycle from concept to competitive selection, prototyping, fabrication, testing, dataset creation, and technology transition; ensuring rapid movement from idea to market-ready solution.
Shared National Facilities Access	Coordinated access to advanced tools and infrastructure; the EUV Accelerator, PPF, ASU Labs, National Labs, Universities, and partner fabs.
Dataset-Centric Research	Embeds AI-ready dataset creation and standardized reporting into every project, enabling reproducibility, transparency, and cross-project learning.
Research Agenda	Aligns funding and project selection with national priorities and grand challenges. Informed by a competition of ideas, workshops, RFIs, and technical advisory board. Goes beyond established industry paradigms and prioritizes problems that would not be addressed through normal business processes.
Technical Advisory Board (TAB)	Provides strategic guidance from leaders across the global semiconductor ecosystem, representing companies with a combined market capitalization exceeding $7 trillion. Chaired by Natcast SVP of Research.
World-Class In-House Expertise & Program Management	Combines deep semiconductor, Advanced Packaging, AI expertise, global research networks, OTA-enabled flexible funding, and scalable program management to maximize technical and economic impact.

Investment to Date

Investment	Details
3,000+ work hours to develop Research Agenda	• Advances grand challenges; achieving 1,000× AI data center performance and efficiency by 2035 and establishing U.S. leadership in AI chips. • Developed through 100+ ecosystem engagements and 3,000+ work hours.
3,600+ work hours in strategy and partnership development	• Established key partnerships within industry to drive Research Agenda. • International Collaborations: IMEC (Belgium), CEA-Leti (France), Fraunhofer (Germany), Tyndall (Ireland), Lukasiewicz (Poland), IUNET (Italy), LSTC, METI (Japan). • Reviewed $1B+ research project proposals.
18,000+ work hours in research program development	• Delivering reproducible datasets via standard test vehicles and benchmarking framework. • Programs Include AIDRIFC, TVIP, BOLD, WIRE, and internal research projects; AI assisted Failure Analysis and next-generation OPC models.

Relevant In-House Expertise

Team Size	Avg Years Relevant Experience	Advanced Degree Holders	Team-wide Accomplishments
24	22	20	World-class semiconductor and materials science experts with deep expertise across the technology stack, from device physics and process integration to AI-driven design, packaging, photonics, and emerging memory.

Subdivision Name	Description
R&D Team	• 11 Ph.D.s, 4 M.S. graduates, 500+ years of industry experience, 525+ U.S. patents. • 1,000+ top-tier peer reviewed publications and 40+ major awards, with decades of leadership in industry, government, and academia. Managed 500+ researchers in multi-institutional collaborations, delivering groundbreaking innovations that advance U.S. semiconductor leadership.

AI-Focused Semiconductor Research

Value to the Nation: Accelerating Chip Innovation Through AI and Data at Scale

Asset type:
- ☑ Driving Speed to Innovation
- ❑ Accelerating Ecosystem Development
- ❑ Solving the Workforce Gap

Value Overview

A portfolio that addresses both sides of the AI–semiconductor equation:
- Using AI/ML to accelerate and optimize semiconductor R&D.
- Developing the next generation of AI hardware, chips, architectures, and systems, to maintain U.S. dominance in AI computation.

Incorporates the Design Enablement and AI-enabled EDA tools, creating a unified approach to AI in design, manufacturing, and system architecture. With aggressive, targeted research aimed at improving AI data center performance by 1,000× and re-establishing U.S. leadership in AI chip manufacturing, this portfolio is integral to national competitiveness.

Components

Component	Description
AIDRFIC Program	Uses AI/ML, large language models, and reinforcement learning trained on comprehensive RF, analog, and mixed-signal design datasets, to streamline RFIC design, reduce errors, and discover novel architectures.
SMAP Program	Develops domain-specific architectures, such as AI accelerators and memory subsystems optimized for power, performance, and area, using extensive benchmark and application datasets for trade-space analysis and the creation of custom programming models.
STCO Framework	A holistic, AI-driven semiconductor design approach that aligns innovations across the technology stack to optimize performance, power, area, and cost, addressing bandwidth, efficiency, and thermal demands of future AI systems.
Scalable AI Metrology & Failure Analysis	AI-powered multimodal inspection for scalable metrology and failure analysis in advanced semiconductor packaging. Creates benchmark datasets and develop physics informed neural network to rapidly detect, diagnose, and predict failures inline - improving yield, reliability, and AI HW TTM.
National AI Data Center Validation Lab	A full-scale testbed with access to rich, real-world and synthetic AI workload datasets, enabling startups and researchers to validate AI hardware under data center conditions, accelerating adoption and reducing deployment risks.

Investment to Date

Investment	Details
6,250+ hours invested to launch $100M+ programs	• Evaluated 134 concept papers and 68 proposals with 20+ experts for Next-Generation Chip Architecture Program (SMAP). • Reviewed 28 concept papers and 26 proposals with 30+ experts for AI Tools for Accelerating RF Integrated Circuit Design Program (AIDRFIC).
150+ hours to define this STCO Framework	• Strategy for developing holistic NSTC Member-driven solution into common framework with reference architectures, informed by industry.
140+ hours in Data Strategy for AI-driven Semiconductor Research & Technical Centers	• Established strategy for national-scale rich dataset repositories for AI/ML semiconductor R&D. • Defined secure data-sharing framework between academia, startups, and industry, including pipeline for enabling federated learning. • Developed strategy for National AI Data Center Validation Lab.

Relevant In-House Expertise

Team Size	Avg Years Relevant Experience	Advanced Degree Holders	Team-wide Accomplishments
11	24	8	Launched $100M+ AI-driven semiconductor R&D to accelerate chip design, advance next-gen AI hardware, and target 1,000× data center performance gains.

Subdivision Name	Areas of Expertise
R&D Team	AI-driven Semiconductor R&D, System Technology Co-Optimization (STCO), RF/Analog/Mixed-Signal IC Design, Domain-Specific AI Architectures, and AI-enabled EDA Tools, Managing $100M+ Research Programs in Private Industry and Federal Agencies.

Natcast

Test Vehicle Innovation Pipeline

Value to the Nation: Accelerating next-generation chips through shared U.S. innovation platforms

Asset type:
- ☑ Driving Speed to Innovation
- ☑ Accelerating Ecosystem Development
- ☑ Solving the Workforce Gap

Value Overview

A cornerstone of Natcast's mission to democratize access to advanced semiconductor prototyping. By providing shared, reusable, and standardized test structures along with partially fabricated wafers, TVIP reduces non-recurring engineering (NRE) costs for new device validation by a factor of 100 – 1000x and shortens prototyping cycles by 6–15 months. Capabilities delivered through U.S.-based facilities, replacing what was previously only available overseas. Each wafer run generates AI-ready datasets, distributed to innovators, building a powerful national resource for AI-driven chip design, manufacturing optimization, and failure analysis. As a gateway to industrial-grade process platforms, TVIP opens the door for universities, startups, and small manufacturers to participate in cutting-edge semiconductor R&D, leveling the playing field for domestic innovators.

Components

Component	Description
Reusable Masks & Common Process Sets	Shared reticle sets and PDKs that allow multiple researchers to share fabrication runs, lowering costs and increasing throughput.
Partially Fabricated Wafer	Wafers with baseline process layers completed, and distributed to innovations nationwide, allowing insertion of new materials, device architectures, or interconnect schemes at specific layers.
Wraparound Metrology & Automated Measurement	Comprehensive electrical, optical, and structural characterization integrated into prototyping pipeline to deliver standardized datasets.
Standardized Modeling	Linking process and device simulation tools directly to experimental data for faster design iterations.
Benchmarking Repository	Curated, anonymized performance data across projects to enable cross-comparison and AI training.

Investment to Date

Investment	Details
4,388+ work hours in First General-Purpose $70M+ TVIP Program launch	• Established foundational model bringing advanced-node technology to innovators through test vehicles, in partnership with foundries and tool suppliers for early- to late-TRL processing, benchmarking, and validation. • 180+ total reviews completed: 78 concept papers, 34 full proposals, $325M+ funding requests
1,522 work hours in $150M+ of additional Test Vehicle Programs for novel materials ready for launch	• Extended TVIP to lower semiconductor stack, enabling novel interconnect and next-gen transistor materials, a first-of-its-kind U.S. offering pathways for energy efficient chips for next-gen AI hardware. • Programs informed by 75+ RFI responses from academic and industry. • Research topics finalized and ready for competitive solicitation.

Relevant In-House Expertise

Team Size	Avg Years Relevant Experience	Advanced Degree Holders	Team-wide Accomplishments
6	22	4	Launched first-of-its-kind U.S. platform that cuts semiconductor prototyping costs by 100×, shortens cycles by up to 15 months.

Subdivision Name	Areas of Expertise
R&D Team	Combined decades of experience in test vehicle design and research at U.S. semiconductor companies such as Intel, NXP, Freescale, and Motorola, with a strong record of international collaboration. Team member served as former Chair of the IEEE International Conference on Microelectronic Test Structures (ICMTS).

EUV Accelerator

Value to the Nation: $825M+ Bringing World-Class EUV Capabilities to American R&D

Asset type:
- ☑ Driving Speed to Innovation
- ☑ Accelerating Ecosystem Development
- ☐ Solving the Workforce Gap

Value Overview

Provides NSTC members with rare, affordable access to U.S.-based extreme ultraviolet (EUV) lithography capabilities, including a leading-edge 2nm process and both standard- and high-NA toolsets. By also investing in next-generation light sources, such as free-electron lasers (FEL), and hyper-NA micro-exposure tools. This investment is pushing the boundaries of semiconductor scaling and precision and serves as a national that resource removes the cost barriers that have long limited access to EUV technology, enabling broad participation in cutting-edge R&D, accelerating innovation, and strengthening U.S. leadership in next-generation semiconductor manufacturing.

Components

Component	Description
Exclusive Facility Access & On-Site Expertise	Secures EUV tool time, dedicated wafer runs, and on-site technical expertise, leveraging both EUV and non-EUV capabilities for advanced semiconductor R&D.
Active R&D Pipeline	Projects include nanosheet FET tuning, EUV resist characterization for NSTC Member datasets, digital twin development using EUV processes, resolution enhancement techniques, and quantum device exploration (Majorana). Future program integration include $150M+ of novel materials research.
Industry & Government Collaborations	Partnerships span leading semiconductor and materials companies and government/academic programs, including NIST-Metrology (CHIPS-M), OPC design projects, and joint research with IBM/NY CREATES and resist vendors.
Next-Generation EUV & Light Source Development	Advancing beyond current EUV capabilities with investments in Hyper-NA tools, alternative light sources such as free-electron lasers (FEL), and programs like TVIP, SMARTUSA, and CHIPS-M to push the boundaries of scaling and precision.
Unique Data Ownership & Analytics	Ownership of in-line metrology, defect, and electrical data, including measurements from direct wafer probing at multiple process stages, creating a dataset for process optimization, modeling, AI-driven research and future R&D.

Investment to Date

Investment	Details
3,720+ hours and $910K+ in EUV Accelerator Program Development	• 1,900+ hours to develop strategy and negotiate contract. • 720+ hours spent building collaborations and partnerships to grow pipeline. • Si wafers currently in process ($860k). • EUV Accelerator specific routes for access security (>100 work hours). • Project Work Scope generation (>1000 work hours). • EUV Accelerator Launch Activities (>$50k).
$180K in EUV Facility Investment	• Office Lease ($20K). • Office Insurance ($50K). • Office Equipment: IT/Server, AV, furniture, supplies (>$100K).

Relevant In-House Expertise

Team Size	Avg Years Relevant Experience	Advanced Degree Holders	Team-wide Accomplishments
6	22	4	Rapidly transitioned from concept to operational reality, securing strategic agreements, building a robust R&D pipeline, and initiating high-value silicon processing for NSTC members.

Subdivision Name	Areas of Expertise
EUV Accelerator Team	Decades of experience at IBM, Intel, GlobalFoundries, AMD, Freescale, Photronics, and top research institutions. Expertise in nanosheet integration, EUV lithography, BEOL process integration, nanofabrication, AI/ML for manufacturing, quantum sensing, photonics, advanced metrology, and failure analysis. 240+ publications, 50+ patents, and a track record of pioneering industry firsts—from the Ne^+ gas field ion source. The team collectively has led multi-institutional programs that shape national R&D priorities and drive next-generation EUV technology from concept to manufacturing.

Advanced Packaging & Photonics

Value to the Nation: Revolutionizing Chip Performance and Energy Efficiency

Asset type:
- ☑ Driving Speed to Innovation
- ☑ Accelerating Ecosystem Development
- ☐ Solving the Workforce Gap

Value Overview

Creating advanced packaging capabilities vital to U.S. semiconductor leadership, delivering innovations in ultra-fine pitch 3DIC, wafer bonding, layer transfer, and heterogeneous integration of memory, high-speed photonic interconnects, and co-packaged optical engines, alongside advanced power and thermal solutions. These technologies enable new material options for CMOS + X, spanning photonics, quantum, RF, and memory innovations, supported by proposed CMOS + X mini-corridor at ASU, designed with dedicated space and facilities to accelerate cross-domain integration. Solutions address critical limits such as the memory wall and data transfer bottlenecks, enabling faster, more energy-efficient AI and high-performance computing. Building domestic lab-to-fab pathways, silicon prototyping capabilities, and robust industry-academic collaborations.

Components

Component	Description
Adv. Packaging & Photonics Research Agenda	Identifies priority research topics in advanced packaging, emphasizing ultra-fine pitch 3DIC to enable pseudo-monolithic integration of innovative materials, novel chiplet partitioning strategies, and advanced design methodologies. Priorities include enhancing thermal extraction systems, integrating advanced power delivery networks, and embedding components to overcome thermal and performance limitations. As part of a targeted strategy to break through the AI performance and energy efficiency bottleneck (“memory wall”), Natcast is advancing 3DIC integration of stacked memory and logic through silicon prototyping and design enablement for advanced packaging–based memory stacking. This strategy aims to create a robust domestic ecosystem for high-speed photonic interconnects, including Co-packaged Optical (CPO) engines, to eliminate data transfer bottlenecks and position the U.S. at the forefront of next-generation AI, high-performance computing, and heterogeneous integration.
Adv. Packaging Process Flow	Advised on a baseline hybrid bonding packaging process flow to serve as a foundation for advanced packaging R&D in the U.S. This includes creating comprehensive tool lists to evaluate and integrate new capabilities, ensuring alignment with national manufacturing priorities. The process flow framework supports scaling innovations from research labs into high-volume domestic production, securing critical semiconductor supply chains.

Investment to Date

Investment	
600+ work hours in establishing internal research and joint-development opportunities	• Established ASU as an internal research hub for a lab-to-fab coupon line, integrating Natcast research output into 300mm manufacturing lines. • Formed three joint-development opportunities with startups. • Provided technical guidance on the SHIELD program through discussions and workshops. • Developed an internal research proposal for a novel low-k chip-to-substrate interconnect material.
500+ person hours in evaluating industry recommendations	• Hosted a 3DIC workshop with industry, academic, and federal research institutions to establish national priorities for heterogeneous integration. • Received and analyzed over 60 RFI submissions from industry to assess potential research programs, ecosystem needs, and infrastructure drivers for Co-packaged Optical (CPO) engines.

Relevant In-House Expertise

Team Size	Avg Years Experience	Advanced Degree Holders	Team-Wide Accomplishments
8	20	7	Establishing key research partnerships, developing strategies for 3DIC memory stacking and co-packaged optical engines.

Subdivision Name	Areas of Expertise
Advanced Packaging & Photonics Team	Advanced packaging, chiplets, STCO, memory stacking, BEOL integration, and heterogeneous integration, with strengths in technology development, high-volume manufacturing transfer, yield optimization, cost reduction, supply chain management, facility implementation, and design for manufacturability. Pioneered breakthroughs in integrated dual damascene processes, fine-pitch organic interposers, advanced ion beam and photonics systems, chiplet ecosystem strategies.

Accelerated, Industry-Driven Workforce Training

Asset type:
- ❑ Driving Speed to Innovation
- ❑ Accelerating Ecosystem Development
- ☑ Solving the Workforce Gap

Value to the Nation: Scaling enrollment in domestic workforce programs approved by employers to train enough American workers to support the expansion of semiconductor design and production in the U.S.

Value Overview

Informed by guidance from senior leaders from dozens of top semiconductor companies, Natcast's workforce initiatives expand effective training, like apprenticeships and certificate programs, and advance training outcomes using new tools, like AI, AR/VR, and online education. Launched programs to support ~9,000 individuals entering/advancing careers and address critical semiconductor talent gaps across the country.

Components

Component	Description
Workforce Advisory Board (WFAB)	Advisory board of senior leadership from top U.S. semiconductor companies and their education/training partners, including VPs and Presidents from Micron, TSMC, Northrop Grumman, Polar, Synopsys, GlobalFoundries, Apple, Samsung, ASU, JFF, Purdue, SEMI, and more.
The TechBridge Program	Providing 400+ people with transportation, mentorship, and other supportive services to increase access to industry training.
Broadening Research and Inter-Disciplinary Graduate Education for Microelectronics Program	Training of BS minors in microelectronics engineering; creation of two new industry-driven curricula: a dual BS plus microelectronic engineering degree pathway; and a microelectronics engineering online certificate program. Anticipated to serve 1,000+
Rapid Semiconductor Skills Development Program	Providing pre-apprenticeship courses and rapid, scalable certificate programs to 400+ entry-level technicians.
WAVE-CHIP Program	Expansion of hardware verification courses to community colleges/universities, and hands-on train-the-trainer courses in hardware verification for 50+ educators + reach of 2,000+ students.
Center for Education of Microchip Designers	New center for training students and engineers in analog and chip design through tape-out classes, providing education to 25+ professors across the U.S. to bring curriculum to 2,000+ students.
Semiconductor Workforce Network	Expanding experiential to 150+ students in community colleges; training 300+ engineers in industry hardware and software skills.

Investment to Date

Investment	Details
2,400+ work hours and $1.7M in 6 employer-approved workforce projects across U.S.	• 6 projects have served 958 learners and workers through July 2025. • Planned to serve an additional 2,000+ individuals by Dec. 2025 without additional investment in award program infrastructure. • Ready-to-deploy, does not require additional delays to implement.
2,500+ work hours in focus groups, surveys, interviews, Communities of Practice, and WFAB meetings	• Immediately deployable custom consulting services offerings for U.S. companies informed by detailed analysis of industry needs. • Up-to-date, synthesized research on current and pressing industry workforce challenges facing over 100+ industry stakeholders that can be used to validate workforce efforts align with real-world needs.

Relevant In-House Expertise

Team Size	Avg Years Relevant Experience	Advanced Degree Holders	Team-wide Accomplishments
12	11	10	• Designed end-to-end flexible and scalable competition processes. • Screened 117 20+ page WFPA applications with an industry expert. merit review panel in less than 27 business days. • Solicited 148 proposals for 2025 Workforce Award consideration. • Assembled 21-member workforce advisory board comprised of industry and academic leaders.

Subdivision Name	Areas of Expertise
Workforce Award Management	Program evaluation, performance monitoring, sector-based workforce strategies, competitive award program administration, merit reviewer training, fundraising.
Workforce Stakeholder Management	Advanced manufacturing services, event planning, board management, apprenticeship supports, education and training systems, focus groups, surveying.
Finance & Legal	Contracting, compliance, audit, ethics, invoicing, fixed-cost awards.

Cutting-Edge Workforce Development Research

Asset type:
- ❑ Driving Speed to Innovation
- ❑ Accelerating Ecosystem Development
- ☑ Solving the Workforce Gap

Value to the Nation: Maximizing visibility and adoption of workforce strategies that are proven to support growth and innovation in the domestic semiconductor industry

Value Overview

In addition to increasing training numbers nationwide, meeting industry workforce needs requires understanding the landscape and improving programs accordingly to prepare students for changing industry needs. Built on deep-rooted industry feedback channels, tailor-made data collection technologies, and domain-specific expertise in advanced labor market analysis, Natcast's workforce research capacity is expansive, informed by the latest trends and challenges reported by employers, and developed to provide actionable information.

Components

Component	Description
Custom-Built Workforce Data System	Foundational data platform built in cooperation with CPO to study the effectiveness of existing workforce development solutions. Allows recipients of funding to register as users and record/manage workforce solution data for research projects securely and effectively.
Deployable Workforce Research Team	Conduct quantitative and qualitative studies on industry workforce topics, produce sector-specific reports and skill gap analyses to inform workforce planning. Generate actionable labor market intelligence and workforce insights and data sets to enable employers to deploy workforce resources. Study education/workforce development programs for effectiveness and make information accessible for policymakers.
NSTConnect Digital Resource Library & Forum	Industry-specific digital resource library and community platform to support semiconductor workforce development. Trusted source for high-quality resources, including training strategies, instructional materials, and best practices. Provides Members with access to wide range of materials; fosters engagement and collaboration through discussions and surveys.

Investment to Date

Investment	Details
2,430+ work hours and $2.98M in custom workforce system design, configuration, and prototyping	• Custom system to track and study workforce intervention effectiveness, including work supported by DoC semiconductor sector investments. • Ready to deploy MVP, pending only finalization of terms of use. • Full system development is more than 80% complete. • Informed by comprehensive weekly planning with CPO regarding workforce investment longitudinal research needs.
2,500+ work hours in configuration, planning and digital resource library content curation	• Digital community engagement platform and library for semiconductor workforce professionals pre-populated with 70+ high-quality resources. • Configured, tested with industry users, terms of use developed, and community guidelines and monitoring framework in-place. • Branding configurable, ready for immediate launch.

Relevant In-House Expertise

Team Size	Avg Years of Relevant Experience	Advanced Degrees	Team-wide Accomplishments
7	17	5	• Led by Former Texas Workforce Commission Chief Analytics Officer. • Developed custom cloud-based workforce data system MVP in 5 mos. • Curated 70+ digital industry workforce best practice resources. • Published interactive dashboard on the flow of talent from postsecondary institutions nation-wide to roles in the industry

Subdivision	Areas of Expertise
Workforce Research Team	Longitudinal research, scenario modeling, micro and macro economics, data visualization, program evaluation, advanced statistical research, multiple regression analysis, cluster analysis, focus groups, skill-level analysis, career pathing, federal datasets, state workforce development systems.
NSTConnect Team	Community & content management, demand gen, forum moderation, business analytics.
Workforce IT	Data visualization, cloud-based data infrastructure, product development backlog and sprint management, database management, DevOps, IT vendor management.

Semiconductor Innovation Fund (SIF)

Value to the Nation: Creates a Flywheel of Innovation through Public-Private Partnership

Asset type:
- ☑ Driving Speed to Innovation
- ☑ Accelerating Ecosystem Development
- ☐ Solving the Workforce Gap

Value Overview

Over the past two decades, private sector funding for semiconductor startups in the U.S. has declined sharply, in stark contrast to rising investment trends in China. Meanwhile, the exponential demand for AI compute is intensifying the need for breakthrough innovation across the semiconductor value chain. To meet this challenge, a robust public-private partnership is essential—both to catalyze early-stage funding in the US and to build strong syndicates that can support startups as they scale.

Components

Component	Description
Deal Pipeline	Team's deep expertise and strong networks across corporate and financial venture capital, combined with its credibility with both founders and funders, has generated a robust pipeline of high-value deals spanning AI infrastructure, AI-driven EDA, co-packaged optics, and other critical technologies.
Platform Structure	SIF Platform is designed to reinvigorate the semiconductor startup ecosystem by bridging funding gaps and attracting both entrepreneurs and investors. The Horizon Fund backs founders at the pre-seed and seed, while the Acceleration Fund drives first institutional rounds, creating a strong pipeline across the funding stack to scale startups.
Investment Structure	SIF investment structure is uniquely founder/syndicate friendly, targeting 10-25X private sector capital leverage for companies raising follow-on rounds; with long term goal of becoming a self-sustaining fund through performance and capital recycling.
Wraparound Services	SIF will leverage NSTC infrastructure to deliver design services that reduce startup operating costs and shorten time to milestone.
Ecosystem Experts	Utilizing the Natcast organization's expertise, SIF can leverage deep sector and technical insights that are either too costly, time intensive, or unavailable to other managers.

Investment to Date

Investment	Details
1,500 work hours to establish credibility, generate strong deal flow, and manage pipeline	• Network of 100+ financial VCs and Corporate VCs developed, vetted, and engaged to collaborate with SIF. • Pipeline of 60+ semiconductor deals (referred to us by financial VCs, Corporate VCs and direct reach). • >60% of deal flow address infrastructure development for AI, with strong Photonics component. • Strong AI for design, photonics, advanced packaging, power delivery.
250+ work hours to develop investment infrastructure	• Affinity deployed for relationship management, deal flow, and investment process. • Legal framework, term sheet and side letter templates developed. • Comprehensive diligence process and deal documentation.

Relevant In-House Expertise

Team Size	Avg Years Relevant Experience	Advanced Degree Holders	Team-wide Accomplishments
5	27	4	• Developed a pipeline of 60+ deals and 100+ syndicate investors. • Lead investors at a top-tier global financial VC, major semiconductor CVCs, and NSF.

Subdivision Name	Areas of Expertise
Investment Team	70+ years of collective experience in semiconductor technology development, engineering and translational research. 65+ years of collective investment experience at top global financial VC, top tier CVCs and NSF, conducting deal sourcing, due diligence, financial modeling, term sheet negotiation and building successful syndicates.
Legal & Support Team	Deal flow management, fund structure and administration, performance tracking, compliance and audit, deal documentation, IP and data protection.

Design Ecosystem Enablement

Asset type:
- ☑ Driving Speed to Innovation
- ☑ Accelerating Ecosystem Development
- ☑ Solving the Workforce Gap

Value to the Nation: Reduces time and cost from concept to prototype by creating a platform offering EDA tools & IP access, silicon aggregation, and test lab - a national asset available to academia and industry

Value Overview

Aims to reduce cost and speed up the semiconductor design lifecycle by 30% and provides 100+ R&D entities with "0 to 1" capabilities they currently cannot access without the NSTC, dramatically increasing national innovation throughput. The platform includes tool and IP access in the cloud, silicon aggregation with predictable MPW shuttle access, and wraparound services. This platform will be a national asset advancing innovation within startups, academia, collaborative R&D, and SMEs; and will put US at par or ahead of the support provided to this strategic sector by China, India, EU, Taiwan, UK & Japan.

Components

Component	Description
Trusted Relationships with EDA Executives	• Long history of creating and running support teams – essential for helping reduce their cost to EDA industry for enabling our members. • Proven ability to engage with very large number of customers and helping them with EDA tools, infrastructure and services. • Trusted connections with senior executives at these vendors.
Deep Technical Partnerships with Foundries	• Extensive experience in multiple process nodes from tier-1 foundries. • In-house talent to become the first MPW aggregator for Intel 18A node. • US mainstream and defense foundry know-how along with strong professional connections.
Design Enablement Gateway (DEG)	• Expertise in chip design and associated cloud infra development. • Expertise in design verification across a broad range of design types up to full system models including emulation/FPGA prototyping. • EDA and cloud vendors aligned with our DEG use model.
Silicon Aggregation (SiAgg)	• Deep legacy & advanced node tape-out experience with Tier-1 foundries. • Experience includes utilizing various technologies & hybrid bonding/3D packaging to the forefront of innovation & product realization. • Tentative collaboration agreements created with other aggregators.
Test & Validation Lab (Dry Lab)	• Expertise in accelerating prototype validation & system-level testing. • Deep experience managing a network of labs facilitating bring-up of test-chips for AI, CPU, GPU, IoT & networking SoCs and IPs.

Investment to Date

Investment	Details
2,000+ work hours to develop GTM strategy and business model	• Development of product strategy, iterating terms and pricing with EDA vendors, foundries, cloud providers, and DOC leadership. • Designed hybrid cloud with specialized hardware for HAV; extensible to purpose-built AI lab/data-center for rapid prototyping of new hardware.
3,300+ work hours to develop infrastructure	• 2,500+ hours architecting & designing product and cloud infrastructure. • Dedicated 800+ hours to capturing requirements, architecting and designing a state-of-the-art lab infrastructure, and curating cutting-edge test instrumentation.

Relevant In-House Expertise

Team Size	Avg Years Relevant Experience	Advanced Degree Holders	Team-wide Accomplishments
11	**26**	**9**	• Created pipeline of 30+ startups to use the design ecosystem enablement platform in 2025/26. • Terms finalized with two EDA vendors and two foundries; completed dry lab architecture.

Subdivision Name	Areas of Expertise
Tool Enablement	• 60+ years experience in semiconductor design and validation. Extensive work with global semiconductor ecosystems supporting tool deployments, methodology development, and tool innovation.
Silicon Aggregation	• 75+ years experience with major fabless semiconductor companies and DIB; Led to billions of chip tape-outs with Tier-1 foundries and packaging houses. Extensive experience has brought advanced nodes and 3D/Chiplet packaging to the forefront of innovation and product realization.
Infrastructure Development	• 40+ years experience in repaid system level test and validation and lab management. • Cloud meeting various requirements for all personas.

Natcast